Schematic Design Request

1. Document Information

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3. Introduction

Purpose of document

The purpose of this document is to establish a consistent set of naming conventions, schematic attributes, and documentation standards for schematic design. These standards should ensure that all our schematics contain the information required for schematic review, hardware debugging, software development, and design reuse.

Guidelines for use of document

This document should be used by the hardware designer in the development and inspection of schematics, and by the hardware debugger and tester in the interpretation of same.

4. General Schematic Guidelines

1. The Cadence EDA Tool is preferred for all schematic designs.
2. Schematics must use the C size Template.
3. Schematics must be available when printed on 11 x 17 paper. (8.5 x 11 in. is also good).
4. Schematics must include clear off page references.
5. Schematics must contain a revision date updated with ANY schematic change.
6. Bypass capacitors should be included on the page with the components they bypass.
7. Terminating resistors should located on the schematic near the components they will be physically placed near.

5. Component Symbol Guidelines

Every electrical component will have one or more symbols (more than one version) on the schematic to represent its connectivity.

1. Resistor symbols will contain an indication of their value in ohms with the suffix ‘K’ and ‘M’ indicating K-ohms and M-ohms respectively, a power rating that will always have a ‘W’ or ‘mW’ suffix for watts and milli-watts respectively, and a required tolerance that will always have a ‘%’ suffix.
2. Capacitor symbols will contain an indication of their value in micro-farads or optionally pico-farads (with a pF suffix), and voltage rating that will always have a ‘V’ suffix. Tolerance will default to 10% unless otherwise indicated.
3. Fixed voltage regulating devices (e.g. linear regulators, zener diodes) will have an indication of their voltage rating, tolerance, and power rating with the suffixes ‘V’, ‘%’, and ‘W’ or ‘mW’ respectively.
4. Adjustable voltage regulating devices will have an indication of their tolerance and power rating as described above, and will be accompanied on the schematic with a note indicating the configured voltage.
5. For FPGA related with several other chips, the pin name label should include the related other chip model name by “_other chip model name”, for example: INIT_VSC9182.

When a schematic note is included in a prominent place identifying a common voltage rating, power rating, or tolerance, these values may be omitted from conforming components.

6. Net Naming Conventions

1. Netnames will contain only upper case alphabetic, numeric, and underscore (‘_’) characters.
2. Signal names should be descriptive of their function (e.g. MAC_I2C_SDA instead of M_PB27).
3. Where it is inconvenient to implement item 2 above, a schematic note describing the function of the generically named signals must be provided.
4. Active low signals must contain “_L” as the last two characters of the netname.
5. Pair routed signals must be constructed of a basename followed by “_P” for the positive signal, and “_N” for the negative signal.
6. The use of “_L”, “_P”, and “_N” as the last two characters in a symbol name will be reserved for the signal types described above.

7. Net and Pin Attributes

Net and pin attributes provide a mechanism for conveying layout and routing requirements both for the schematic inspection and for hardware implementation.

1. Net attribute “SL” will be used to indicate a short net length for component placement purposes (e.g. this attribute will be placed on the net connecting a clock output to it’s series terminating resistor).
2. Net attribute “CI” will be used to indicate routing on a controlled impedance layer.

3. Pin attributes “S”, “L”, and “T” will be used to indicate source, load, and termination and will drive “ECL” style net routing (i.e. the route will have the “S” and “T” pins as it’s end points, and the “L” pins will be through routed with no net stubs, or minimal length net stubs if required for device fanout). A net will contain no more than one pin with an “S” attribute. Two “T” attribute pins may be used in the case of thevinin terminations.
4. Net attribute “C” will be used to identify nets constrained in some other fashion, which will be documented with a schematic note.

8. Component Attributes

1. Attribute “DNI” will be used to indicate “Do Not Install” components. These components will not appear in the bill of materials and will not be installed. This attribute is provided for configuration resistor, dual footprint and alternate component situations (e.g. crystal vs. crystal oscillator). When the “DNI” attribute is attached to a component, all otherwise identifying component information (e.g. resistor value) is still required.
2. Attribute “MO” will be used to indicate “Models Only”. These components will only be installed when building engineering models (e.g. test headers, programming headers not required for production). When the “MO” attribute is attached to a component, all otherwise identifying component information (e.g. resistor value) is still required.

9. Descriptive Text

As the schematic is the central point of information for a circuit, additional descriptive text must be provided to support inspection, hardware realization, software development, test, debug, and design reuse.

1. If not explicated by signal name, the function of processor chip selects and general purpose I/O must be described in a note on the page with the controlling device.
2. If not explicated by signal name, the function of all configuration resistors must be described in a note on the page with the configuration resistors. When the function is too complicated to describe in detail, an attempt should be made to summarize, and the note must contain a reference to a document (including the relevant section number) that best describes the function.
3. Where there are component placement, routing, ground plane segmenting requirements, or any other information required by the hardware realization team, not otherwise explicated by netname or attributes, a note must accompany the affected components.
4. The inclusion of additional supporting information such as software address maps, power dissipation estimates, circuit board stackups, and physical design requirements is strongly encouraged.

10. Approvals

10.1. Baselined

10.2. Major revision

11. References