Low-Power Four-Quadrant Multiplier Using Dual-Gate Transistors

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Abstract

A four-quadrant analog multiplier using a novel type of GaAs transistor is presented. This device, called 2-D MESFET, is dedicated to low power and high speed applications[1],[2]. A special architecture for the multiplier was designed by taking advantage of the dual-gate structure of the 2-D MESFET. The circuit relies on the square algebraic identity [8], with the squaring operation realized by transistors in saturation. The fabrication of 2-D MESFET integrated circuits is still in its infancy but successful device prototypes have been fabricated and characterized, and accurate models for the device are available with AIM-Spice. Extensive simulations show correct functionality of the multiplier at high frequencies (30GHz) with low power consumption (0.5mW).

1. Introduction

This paper presents a multiplier based on the square algebraic identity [8], using a novel transistor type called 2-D MESFET [1],[2]. The material used for manufacturing the device, GaAs, as well as its structure, makes it well adapted for low power and high speed applications [3]. One feature of the 2-D MESFET that was not fully exploited until now is its dual-gate configuration. As can be seen in Fig. 1, the 2-D MESFET has four terminals: a source S, a drain D and two gates G1 and G2. Other devices can also be considered with four terminals (e.g. MOSFET transistors have a bulk terminal) but the 2-D MESFET is unique because its two gates are *identical* in functionality. The 2-D MESFET can be used to build an analog four-quadrant multiplier with only four active devices and with very good performance. The influence of non-perfect square law in the saturation region for the 2-D MESFET is analyzed and simulations are used to validate the functionality and the performance of the multiplier.

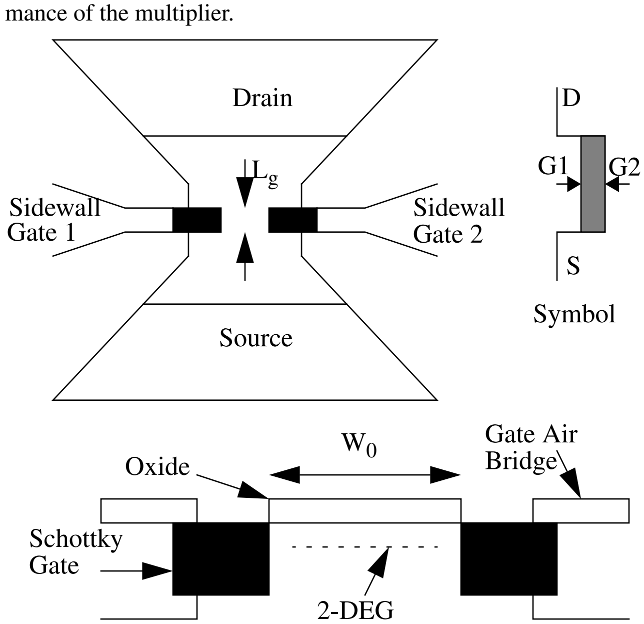

Fig. 1 Top View, symbol, and cross section of a 2-D MESFET

2. The 2-D MESFET dual-gate transistor

2.1. Device description

The transistors used in this paper are called two-dimensional (2-D) MESFETs. They use a two-dimensional electron gas layer in the channel region, which increases the switching speed of the transistor [1],[2]. This feature is also common to HEMTs (High Electron Mobility Transistors) or HFETs (Heterostructure FETs).

The device has two lateral Schottky gate contacts which modulate the width of the 2-D electron gas layer as seen in Fig. 1. These two identical gates have very low capacitances (0.05fF) which also account for the high speed and low power of the device. More detailed physical characteristics of the 2-D MESFET can be found in [1],[2], and [3]. 2-D MESFETs have been successfully fabricated and tested as prototypes in the laboratory but the fabrication of more complex circuits is still in its infancy. In this paper we explore the circuit design space through simulation expecting that 2-D MESFET integrated circuits will be manufacturable in the future.

2.2. Simulation

Accurate models for the 2-D MESFET are available in AIM-Spice [4], which allowed us to obtain the results presented in this paper. The 2-D MESFET model provided with AIM-Spice requires specific parameters and we used parameters that were based on actual measurements on fabricated devices [3], hence the simulations can be considered reasonably close to reality.

When the two gates of the 2-D MESFET are connected together, the device behavior is similar to a regular MESFET, except that it is faster and consumes less current. Fig. 2 shows the 2-D MESFET current-voltage characteristics. The voltage between the two gates and the source was swept between -0.5V (the thresh-

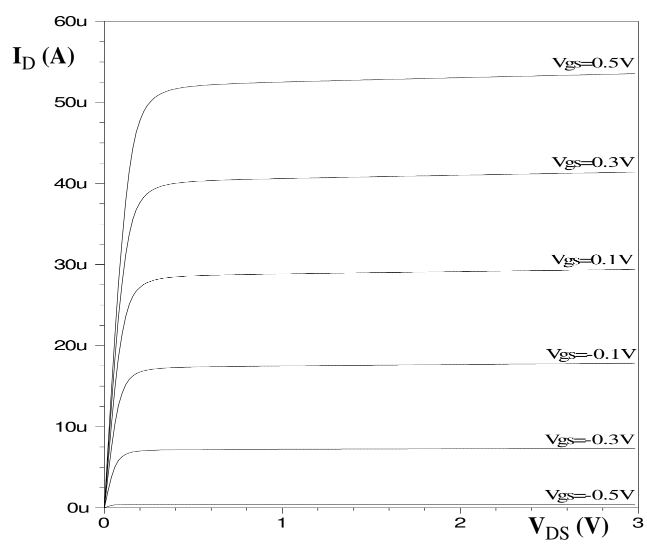

Fig. 2 I-V curves of the 2-D MESFET

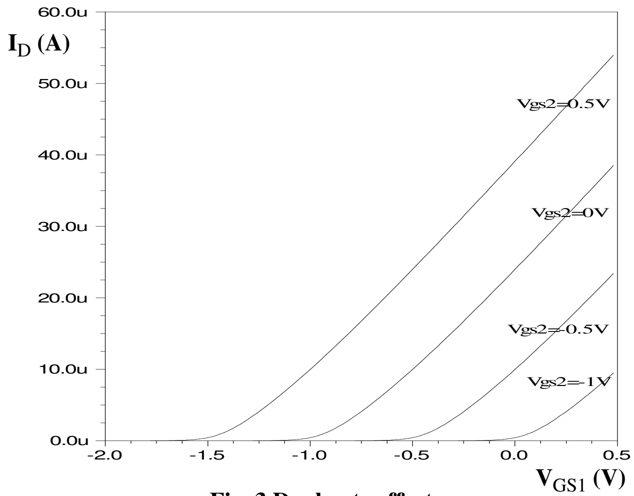

Fig. 3 Dual gate effect

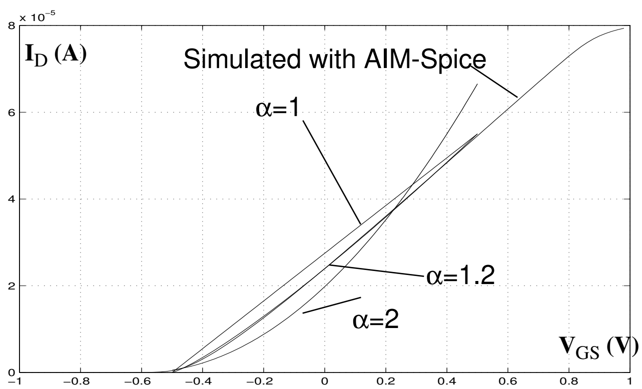

Fig. 4 2-D MESFET α evaluation

old voltage for the transistor) and +0.5V. It can be seen that the drain current is low compared to other FET transistors (uA). Typically this would be a disadvantage for charging and discharging load capacitances, but it is compensated by the 2-D MESFET extremely low gate and parasitic capacitances (around 0.05fF for the gate capacitance). Luckily, the wire parasitics for GaAs are also generally low due to the semi-insulating substrate.

A feature that was not fully explored until now is the independent use of the two gates of the 2-D MESFET. For instance one of the gates can be used to control the threshold voltage as shown in Fig. 3. By applying a constant voltage (V_{GS2}) on one of the gates, the transistor turn-on point can be modified. This property allows the change of the 2-D MESFET behavior from depletion mode to enhancement mode: when V_{GS2} is equal to -1V, the 2-D MESFET is “on” when V_{GS1} is equal to 0V. A similar effect can be obtained for MOSFETs by controlling their “backgate” (or bulk) [6],[7].

Applying two different voltages on the two gates results in the same drain current as applying the average of those voltages to both gates. The saturation current for the 2-D MESFET can be expressed analytically in two different ways, depending on whether the two gates are joned or not:

$$I_{sat} = K \cdot (V_{GS} - V_T)^{\alpha}$$
$$I_{sat} = K \cdot \left(\frac{V_{GS1} + V_{GS2}}{2} - V_T\right)^{\alpha} \qquad (1)$$

where K is the transconductance parameter, V_{GS} the voltage on both gates if they are connected together, V_{GS1} and V_{GS2} the voltage on the gates when they are independent, α a saturation parameter that ideally should be equal to 2, but for real fabricated devices is only slightly larger than 1. A similar α-power law model for MOSFETs was presented in [5]. For the 2-D MESFET, curve fitting experiments show that $K \approx 0.55 \times 10^{-4}$ and $\alpha \approx 1.2$ (see Fig. 4). In the next section we show that multipliers can be built with 2-D MESFETs for α = 2, and debate the influence of a lower α.

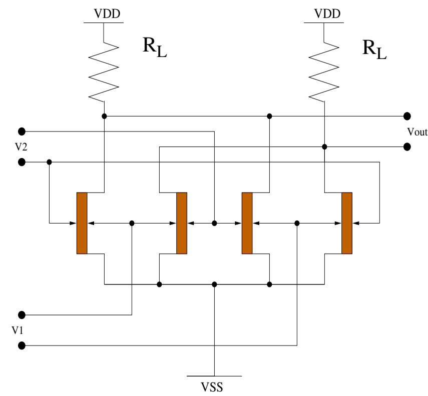

Fig. 5 Novel multiplier using 2-D MESFETs

3. A novel multiplier using 2-D MESFETs

A configuration commonly used in RF mixers and in analog multipliers is the Gilbert Cell [8]. We used the Gilbert Cell as an inspiration for our own circuit shown in Fig. 5. By taking advantage of the 2-gate configuration of the 2-D MESFET our multiplier uses only four active devices (compared to seven for the Gilbert cell).

By choosing the values for VDD and RL, and assuming that the input signals have an amplitude of a few hundred millivolts, we can keep all the transistors in saturation. Using the current formula for the 2-D MESFET (1) we can compute the currents flowing in the resistors, and the output voltage Vout.

To account for different values for α, we evaluate its influence by using Taylor’s expansion applied to 2-variable functions.:

$$f_a(x, y) = a^{\alpha} + \alpha(x+y)^{\alpha - 1}$$
$$+ \frac{\alpha(\alpha-1)}{2}(x^2 + 2xy + y^2)a^{\alpha-2}$$
$$+ \frac{\alpha(\alpha-1)(\alpha-2)}{6} \cdot (x^3 + 3x^2y + 3xy^2 + y^3)a^{\alpha-3}$$
$$+ \ldots \qquad (2)$$

The function f was defined as such in order to simplify the expansion while still corresponding to the saturation current equation (1): to obtain the current in any transistor in the circuit, one only has to multiply *f* by the constant *K*, to replace *x* and *y* by the gate voltages divided by two, and *a* by minus the threshold voltage. Applied to the schematic in Fig. 5, with -0.5V threshold voltage transistors, the following expression is obtained for V_{out}:

$$V_{out} = K \cdot R_L \cdot \left(f_{0.5}\left(\frac{V_1}{4}, \frac{V_2}{4}\right) + f_{0.5}\left(\frac{-V_1}{4}, \frac{-V_2}{4}\right)\right)$$
$$+ K \cdot R_L \cdot \left(f_{0.5}\left(\frac{-V_1}{4}, \frac{V_2}{4}\right) + f_{0.5}\left(\frac{V_1}{4}, \frac{-V_2}{4}\right)\right) \qquad (3)$$

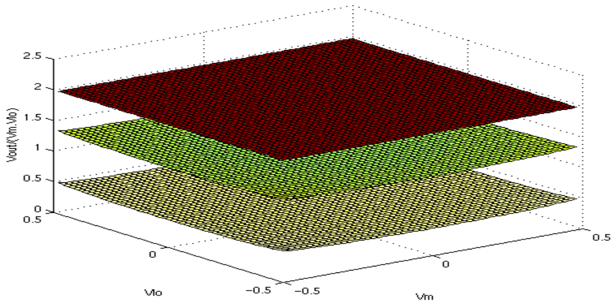

Fig. 6 Effect of factor α (for α=1.2, 1.6 and 2)

An input signal of magnitude V on port 1 or 2 is differentially distributed on the two connections for this port (i.e. V/2 on one connection and -V/2 on the other one), this being the reason why the input voltages are divided by 4 in equation (3). Applying the Taylor expansion from (2) to expression (3), we obtain:

$$V_{out} = K \cdot R_L \cdot \alpha(\alpha-1) \cdot 0.5^{\alpha} \cdot V_1 V_2 + K \cdot R_L \cdot \frac{\alpha(\alpha-1)(\alpha-2)(\alpha-3)}{24} \cdot 0.5^{\alpha} \cdot (V_1^3 V_2 + V_1 V_2^3) + \ldots \quad (4)$$

As can be seen, the even power terms cancel out, and the expansion has to be made until order 4 in order to find the first distortion components, which are the ones that are not strictly proportional to the product $V_1 \times V_2$.

A factor $\alpha = 2$ would make the circuit from Fig. 5 an ideal multiplier according to the square algebraic identity [8], since in that case the formula becomes $V_{out}=2KR_LV_1V_2$. On the other hand, for $\alpha = 1$ V_{out} becomes zero, as all the terms cancel out. Between these two extreme cases, considering that $1 < \alpha < 2$, equation (4) shows that the desired product term will be attenuated as α gets closer to 1 and will be distorted due to the 4th order term, as well as higher order terms not shown above.

Equation (4) allows us to derive the expression of the multiplier's 4th order distortion, which we define here as the ratio of the 4th order term divided by the 2nd order term:

$$Dis = \frac{(\alpha-2) \cdot (\alpha-3) \cdot \left(V_1^2 + V_2^2\right)}{24}$$

For the multiplier's accuracy, keeping the distortion as small as possible is crucial. This can be achieved if the input signals V_1 and V_2 have a low amplitude but this restriction in the input range is typically not desirable for multipliers.

To have a better understanding of the attenuation and the distortion due to α, Fig. 6 shows a plot of $V_{out}/(KR_LV_1V_2)$ for different values of α (1.2, 1.6 and 2). As expected, $\alpha = 2$ gives a plane at z = 0.5, and for the other values the attenuation is obvious, but the distortion is small. In conclusion, for the 2-D MESFET modeled considering α=1.2, which corresponds to measurements and simulation, keeping both input signals lower than 1V results in less than 12% distortion on the output signal, the distortion becoming less than 3% for 0.5V input signals.

In the next section, we examine the characteristics and the limitations of the novel 2-D MESFET multiplier. Extensive simulations with AIM-Spice were done in order to obtain the results.

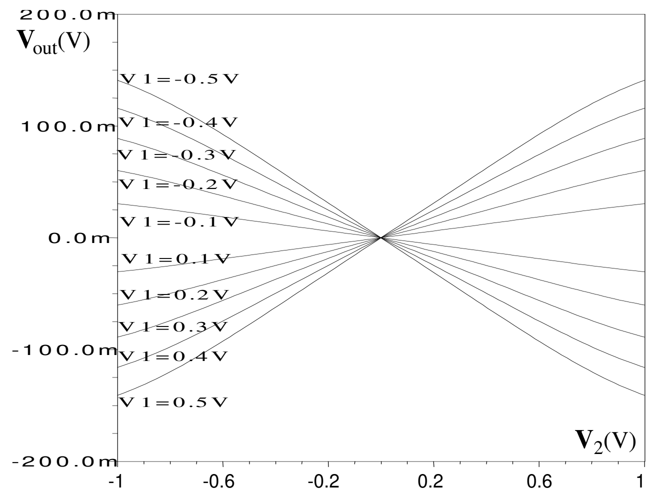

Fig. 7 Static behavior of the multiplier

4. Multiplier Characteristics

4.1. Static behavior

Fig. 7 shows V_{out} while V_2 is swept between -1 and 1V for different values of V_1 (between -0.5 and 0.5V). The value chosen for R_L was 100kΩ and V_{DD} was set to 5V for the simulations. The inflection on the curves obtained show that the multiplier is not perfectly linear for large inputs due to the 4th order distortion, but the expected behavior is achieved. It can be noted that the formula for the output voltage can be approximated by: $V_{out} \approx V_1V_2/3$

4.2. Dynamic behavior

In order to show the dynamic behavior of the multiplier we apply two sine waves of the same magnitude (0.4V) and frequency (10 MHz) on both input ports. We express these signals as being:

Then, according to the relation given in the previous paragraph, the output signal is approximately:

Thus the output signal frequency is twice the input frequency, and it has a non-zero DC value. Fig. 8 shows the FFT of the output with the inputs at 20GHz which verifies the high speed capabilities of the 2-D MESFET. At this high frequency the output signal is more attenuated compared to lower frequencies but the harmonic distortion is still almost invisible on the FFT chart. To evaluate the influence of frequency on the gain and the distortion of the multiplier, we applied a constant signal V1=0.4V on port 1 and a sine wave with a 0.4V amplitude on port 2 at different frequencies. The obtained normalized gain and the ratio of the third harmonic by the fundamental are represented in Fig. 9 (we chose not to investigate further in harmonics, as the simulations showed no second order distortion and negligible higher order harmonics). As one can see, the bandwidth is as high as 30GHz (simulated) and the distortion does not exceed 0.55%. Note that the distortion decreases with input frequencies higher than 15GHz. This is due to the fact that the third harmonic becomes high enough in frequency to be attenuated

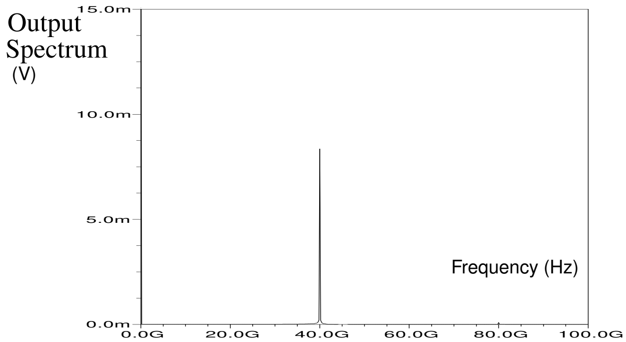

Fig. 8 Dynamic behavior at high frequency.

"naturally" by the circuit parasitics. It has to be noted that our simulations cannot fully take into account the matching and wiring issues that arise at such frequencies for fabricated circuits which may further reduce the performance of the multiplier.

4.3. Summary of results

The following table summarizes the simulated performance of the proposed multiplier:

Table 1: Multiplier simulated performance

Gain	$0.33V^{-1}$
Bandwidth for V_1 and V_2	30GHz
3rd harmonic distortion	0.55%
Input range for V_1 and V_2	0.5V
Power consumption	0.5mW

The gain and 3rd harmonic distortion in the table are valid for signals of magnitude up to 0.5V. It is possible for the multiplier to treat signals up to a magnitude of 1V, but a higher distortion and lower gain will result. The power corresponds to a 30GHz and 0.4V amplitude input signal. We are confident that the simulation results for this fast and compact multiplier will be validated by measurements once the fabrication issues related to building 2-D MESFET integrated circuits are solved.

5. Conclusions

A new topology for building multipliers was shown in this paper. It is based on the use of high speed and low power dual-gate GaAs transistors called 2-D MESFETs. A special architecture for the multiplier was designed by taking advantage of the dual-gate structure of the 2-D MESFET. The circuit relies on the square algebraic identity [8], with the (approximate) squaring operation realized by using the transistors in their saturation region.

We believe that the simplicity, compactness, high speed and low power (0.5 mW, even at 30 GHz) should be of interest to analog signal processing designers. The power consumption, along with the bandwidth, are the strong points of this multiplier

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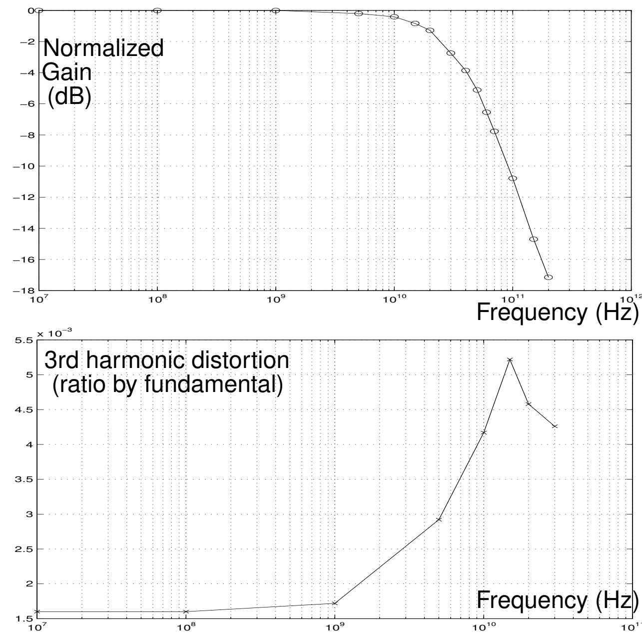

Fig. 9 Normalized gain and third harmonic distortion.

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