Op-amps as “firm” Virtual Components for Systems-on-Chip

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Abstract

We propose a new design methodology for op-amps as “firm” Virtual Components for Systems-on-Chip. A fast time to market, robustness to process variation and process migration, and the fact that most SOC designers are digital designers require a new approach to analog design that is closer to digital methods. Our symmetry-based design method consists of a series of “rules of thumb” that ensure a robust functionality and good performance. The resulting “firm” virtual components are easy to generate by computer, have a regular layout, and can be scaled for different performance levels without the multiplicity characteristic for “hard” components.

1. Introduction

A System-on-Chip (SOC) typically includes both analog and digital Virtual Components (VC) and, although the analog circuits are typically few and small compared to the digital ones, the analog design can become the bottleneck because of several reasons:

- the SOC designers are typically digital designers for which analog design is perceived as “black magic”,
- optimization for analog circuits is not as well defined as for digital ones.

Complex analog circuits are typically generated as “hard” cells with a precise layout in order to account for physical design parasitics [8]. On the other hand, the required performance for analog circuits, especially for generic building blocks like op-amps, can be very different from application to application. This becomes a problem for intellectual property (IP) designers as the combination of hard cell and continuous performance requirements leads to a combinatorial increase in the number of required design variations for the same functionality. This is rarely a problem for digital circuits for which the number of required performance levels is reduced. Furthermore, digital circuits can be delivered as synthesizable “soft” cells which minimizes the number of cells to be designed and delivered.

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Analog circuits cannot typically be delivered as soft cells because of their high sensitivity to placement and routing parasitics. There have been efforts to develop CAD tools for analog design [2, 6] that would be able to “compile” soft cells but until now they have not been widely accepted. As a consequence it is standard practice in industry to only provide (hard) virtual components for *complex* analog blocks which do not require many performance levels. It is assumed that the simpler cells which may need many performance levels are going to be designed in-house [8]. The main argument for this situation is that the simple analog cells are the analog equivalent of simple digital gates and that there si no interest in buying a simple op-amp as IP as there is no interest in buying a 2-input NAND gate, for example. In fact the situation for simple analog cells is very different from the situation for digital gates which have been always available as “books” in standard cells libraries. The same is not true about analog cells as it is difficult to capture all the possible variations and performance levels in a library of predesigned analog components. A library of analog cells should contain cells that are easily parameterizable for desired performance. The method proposed here tries to accomplish this goal by delivering simple analog cells as firm virtual components that are similar to soft cells in the low number of required designs but still approach the accurate parasitic estimation of typical hard cells.

1.1. Op-Amps as Virtual Components

The design methodology presented here is specifically for op-amp design but similar approaches can be devised for other types of analog circuits. The main idea is to come up with a design methodology that combines circuit and layout aspects by constraining the design space such that the resulting behavior is robust, easy to optimize and generate by computer, and the layout is regular and scalable for easy parasitic estimation.

The number of possible circuit *topologies* for an op-amp is relatively small and most are readily available in textbooks [3, 7], but *sizing* and *biasing* these known circuits for different applications results in the undesirable large number of choices. Although op-amps are relatively easy to analyze, their optimization can be complex and can lead to less robust solutions by bringing the design to a corner of

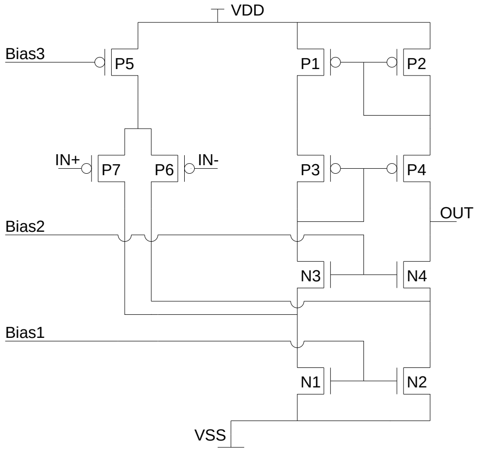

Figure 1. Folded cascode op-amp.

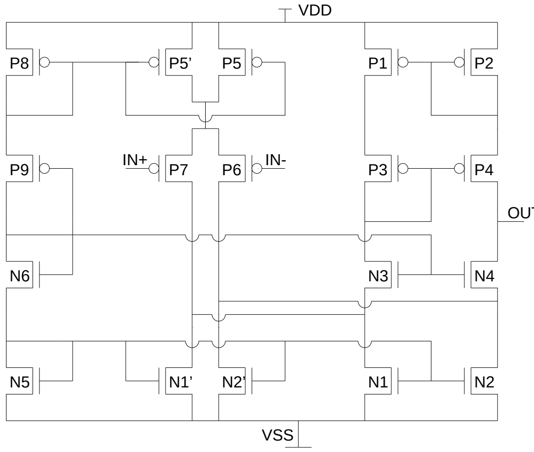

Figure 2. Op-amp with Horizontal and Vertical Matching and matched Biasing.

the design space [4, 5, 1, 6].

Compared to analog, digital circuit design is made simple by the existence of various "rules of thumb": the PMOS transistor is made m times wider than the NMOS for balanced noise margins, where $m = \mu_n/\mu_p$, N transistors in a "stack" are sized N times wider than in the non-stacked case for equal rise and fall times, etc. Such rules of thumb guarantee correct functionality and good performance for digital gates although the performance may not be optimal. Analog circuits in general, and op-amp design in particular, may require a lengthy analysis not only for best performance, but even for correct functionality.

In this paper we propose several analog "rules of thumb" that guarantee correct functionality with good performance for a class of CMOS op-amps. With the proposed methodology, the circuit topology (including biasing circuit) is chosen *a priori* and the only requirement is a correct transistor sizing to optimize performance while satisfying design constraints. The fast design time is suitable for mixed-signal circuits with fast time to market requirements and the method is easy to include in CAD tools with circuit generators for "firm" macros. With a firm virtual component the circuit layout can be determined with enough accuracy to make a good estimation of all parasitics without the disadvantages of having to deal with multiple instances that are necessary for a hard macro approach. The method can also serve as a first iteration for further optimization steps.

2. The Symmetry-based op-amp design method

The folded cascode op-amp shown in figure 1 is the target circuit. The Symmetry-based op-amp design method can be adapted for other circuit topologies but it works best for circuits which intrinsically have a lot of symmetry. With the circuit topology being chosen, the only requirement for the design is to correctly size transistors in order to optimize performance while satisfying design constraints.

The proposed design method is based on a set of "rules" that are extensions and generalizations of explicit or implicit design rules used by analog designers, the novelty consisting in the simultaneous use of all rules at the same time and in optimizing the constrained result which leads to several advantages:

- *Scalability* - The circuit can be easily migrated to different processes while assuring correct functionality,
- *Sizing* - The transistors are easily sized,
- *Biasing* - The biasing scheme is highly tolerant to process variations,
- *Optimization* - Easy optimization for gain, area and power without extensive analysis,
- *Layout* - The layout is simple and regular because of symmetry and can be easily generated by computer,
- *Parameter reduction* - The number of parameters to be optimized is reduced by imposing design constraints.

2.1. Horizontal Matching rule

In a folded cascode op-amp there are 11 transistors to size and 3 biases to be determined for a total of 14 initial parameters. The Horizontal Matching rule asks that the circuit be composed of a number of (almost) identical columns of transistor stacks. Applying the Horizontal Matching rule produces a circuit with (almost) identical columns of transistor stacks, each carrying the same current governed by the biasing network. By using such a topology the transistors are easy to size and the layout becomes regular and compact the Horizontal Matching rule being just an extension of standard mirroring widely used in analog design [2]. From the symmetry we get the following W/L ratios for the circuit (see figure 2):

$$
\begin{gathered}
W/L_{n1} = W/L_{n2} = W/L_{n1'} = W/L_{n2'} \\
W/L_{n3} = W/L_{n4} \\
W/L_{p1} = W/L_{p2} = W/L_{p5} = W/L_{p5'} \\
W/L_{p3} = W/L_{p4} \\
W/L_{p6} = W/L_{p7}
\end{gathered}
$$

There are 5 transistor sizes and 3 biases left to optimize which reduces the number of free variables from 14 to 8.

2.2. Biasing Network rule

The Biasing Network rule asks that the biasing be done with a column of stacked transistors identical to the ones obtained with the Horizontal Matching rule. This ensures that all the transistors are in saturation at the expense of lower performance but with the advantage of robustness to parameter variations. The op-amp schematic becomes as in figure 2 with the sizes for the transistors given by:

$$
\begin{gathered}
W/L_{n5} = W/L_{n1} \\
W/L_{n6} = W/L_{n3} \\
W/L_{p8} = W/L_{p1} \\
W/L_{p9} = W/L_{p3}
\end{gathered}
$$

Using such circuit has the advantage of an implicit biasing in saturation (no need for analysis), tolerance to process variations and a compact and easy layout. It also has the disadvantage of a reduced voltage swing at the output and non-optimal performance by not bringing the design close to a corner of the design space. The number of parameters to be optimized is reduced now to only 5 transistor sizes.

2.3. Vertical Symmetry rule

The Vertical Symmetry rule asks for the W/L of every PMOS transistor to be m times larger than for the NMOS which is mirror-symmetric in the vertical dimension, where $m = \mu_n/\mu_p$ for the given CMOS process. This rule is similar to the sizing rule for complementary static CMOS gates and it ensures a low offset and robustness to parameter variation and results in the following transistor sizes:

$$
\begin{gathered}
W/L_{p1} = m \cdot W/L_{n1} \\
W/L_{p3} = m \cdot W/L_{n3}
\end{gathered}
$$

Using the Vertical Symmetry rule we are left with just 3 free variables: W/L_{n1}, W/L_{n3} and W/L_{p6}. We can fix the size of the $N1$ transistor and express the W/L of the $N3$ transistor as x times that of the $N1$ transistor and the W/L of the $P6$ transistor as x' times that of the $P3$ transistor so that we are left with the following 3 parameters: W/L_{n1}, x and x'. We can constrain the design space even more by making $x' = x(1+1/m)$ for optimum use of area such that all transistor columns have exactly the same height, and we are left with only two parameters: W/L and x.

$$
\begin{gathered}
W/L_{n3} = x \cdot W/L_{n1} = x \cdot W/L \\
W/L_{p6} = x' \cdot W/L_{p3} = x' \cdot m \cdot W/L (= x \cdot (m+1) \cdot W/L)
\end{gathered}
$$

Other parameters which determine the characteristics of the op-amp (e.g. the supply voltage, V_{th}) are typically given and not under the control of the designer. In what follows we are going to use the constrained design space determined by the Symmetry-based design rules in order to optimize the op-amp DC gain, area and current consumption. The gain-bandwidth, slew rate and output swing are not part of the optimization but can be included as constraints. In case the obtained values are not appropriate a separate output stage can be used to independently increase the slew rate and/or the voltage swing. The op-amps presented in this paper have a low bandwidth, as the target application required, but designs with higher bandwidths are possible.

3. Gain for symmetry-based design

The optimization method presented here is a type of equation-based synthesis [6]. The estimated performance can be relatively far from accurate simulation results but we consider this to be acceptable for a virtual component for most applications, where the critical aspects are tolerance to process variations and robustness. Once the sizes have been determined a more accurate simulation ca be performed and the sizes readjusted as necessary with minimum impact on design time due to the simplicity of the design.

The Gain for a folded-cascode op-amp like the one considered here is of the form [7]:

$$
G = \frac{|V_A|^2}{I} \frac{2 \cdot \sqrt{\mu_n \mu_p} \cdot C_{ox} \cdot \sqrt{W/L_{p6}}}{3/\sqrt{W/L_{n3}} + \sqrt{\mu_n/\mu_p}/\sqrt{W/L_{p3}}}
$$

where $V_A = 1/\lambda$ is the *early* voltage [7], I is the current in one of the transistor "columns", V_{th} is the same for both PMOS and NMOS and all secondary effects like body effect, and short channel effects are ignored. Ignoring some of the second order effects is legitimate if the transistor sizes (both W and L) are much larger than minimum size which is anyhow desirable for analog circuits in order to reduce the effect of manufacturing variations.

Replacing the sizes according to the Symmetry-based design rules results in the following simplified formula:

$$
G = \frac{|V_A|^2}{I} \frac{\sqrt{\mu_n \mu_p} \cdot C_{ox} \cdot \sqrt{x} \cdot \sqrt{x'} \cdot \sqrt{m} \cdot W/L}{2}
$$

The current I can be easily determined by analyzing the Symmetry-based biasing network as:

$$
I = \frac{1}{2} \mu_n \cdot C_{ox} \cdot W/L \cdot (V_{dd}/2 - 2V_{th})^2 \cdot \frac{x}{(1+\sqrt{x})^2}
$$

Table 1. Simulated open-loop gain.

W/L_{n1}	10/120	10/60	10/30	10/10
Gain	131dB	91dB	88dB	88dB

Table 2. Transistor sizes for minimum area.

dimension	value	numeric
W_{n1}	w	10
L_{n1}	$l\sqrt{x}\sqrt{m}$	60
W_{n3}	$w\sqrt{x}/\sqrt{m}$	20
L_{n3}	l	10
W_{p1}	$w\sqrt{x}\sqrt{m}$	60
L_{p1}	l	10
W_{p3}	w	10
L_{p3}	$l\sqrt{x}/\sqrt{m}$	20
W_{p6}	$w\sqrt{x}\sqrt{m}(1+1/m)$	80
L_{p6}	l	10

Replacing I into the gain equation we can finally obtain:

$$G = \frac{|V_A|^2\sqrt{x\cdot x'}\cdot(1+\sqrt{x})^2}{x\cdot(V_{dd}/2-2V_{th})^2}$$

For $x' = x(1+1/m)$ the gain becomes:

$$G = \frac{|V_A|^2\sqrt{1+1/m}\cdot(1+\sqrt{x})^2}{(V_{dd}/2-2V_{th})^2}$$

The most interesting aspect of the obtained formula is that the gain is only a function of the *ratios* x and x' but is totally independent of the actual size W/L, which provides an opportunity for independently optimizing gain, area and power consumption (current). For high DC gain x needs to be maximized (and x' if it is an independent variable).

Of course the formula for the gain independent of transistor sizes is only a first order analysis, and simulations show a relative variation in gain for different transistor sizes. Table 1 shows the value for the gain for $x = 12$, $m = 3$, $x' = x(1+1/m) = 16$ together with four values of W/L: 10/120, 10/60, 10/30 and 10/10. Except for the first column which has a higher gain due to the transistors getting into weak inversion the other three columns show almost the same gain.

3.1. Optimizing the area

Since the gain is only a function of the ratio x we can independently optimize the area for a given x. The current is not considered for this optimization although it can be used as a constraint. The area for the op-amp can be estimated as in the following formula (there are 5 almost identical transistor "columns"):
$A = 5\cdot a\cdot(W_{n1}\cdot L_{n1} + W_{n3}\cdot L_{n3} + W_{p1}\cdot L_{p1} + W_{p3}\cdot L_{p3})$

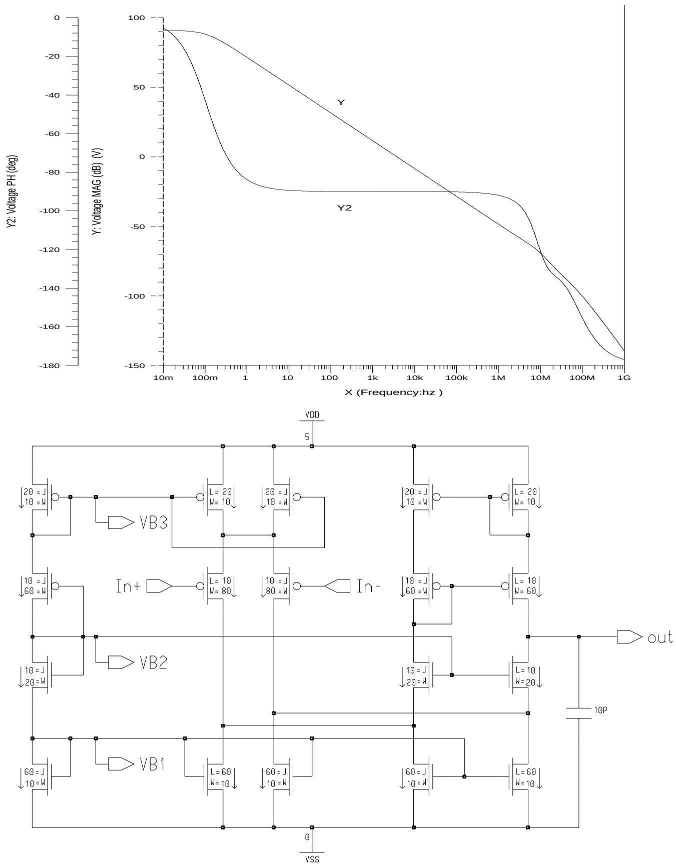

Figure 3. Gain-phase and schematic for optimized area and layout.

where a is a constant, dependent on the layout style and design rules, which is the ratio of the total area to the area for the active region.

The optimization problem becomes:
minimize $W_{n1}\cdot L_{n1} + W_{n3}\cdot L_{n3} + W_{p1}\cdot L_{p1} + W_{p3}\cdot L_{p3}$
subject to the constraints:
$W/L_{n3} = x\cdot W/L_{n1}$
$W/L_{p3} = x\cdot W/L_{p1}$
$W/L_{p1} = m\cdot W/L_{n1}$
$W_i \geq w$ (minimum transistor width for the circuit)
$L_i \geq l$ (minimum transistor length for the circuit)
$x \geq m$ (generally true when a high gain is desired)

The resulting transistor sizes for a given gain are summarized in table 2. Column three shows a numeric example for $x = 12, m = 3, w = l = 10$, which results in the schematic and Bode plot in figure 3 which show good performance and robust phase margin with a 10pF load.

The transistor sizes in table 2 and figure 3 allow a very regular layout. For the given DC gain, the current consumption and total area are much smaller than for the "traditional" sizing approach [7] which uses minimum size transistors for $N1$ and $P1$ and much larger $N3$ and $P3$. By using long transistors for $N1$ and $P1$ we are able to obtain a high gain while balancing the area used by $N1$ and $P1$ with the

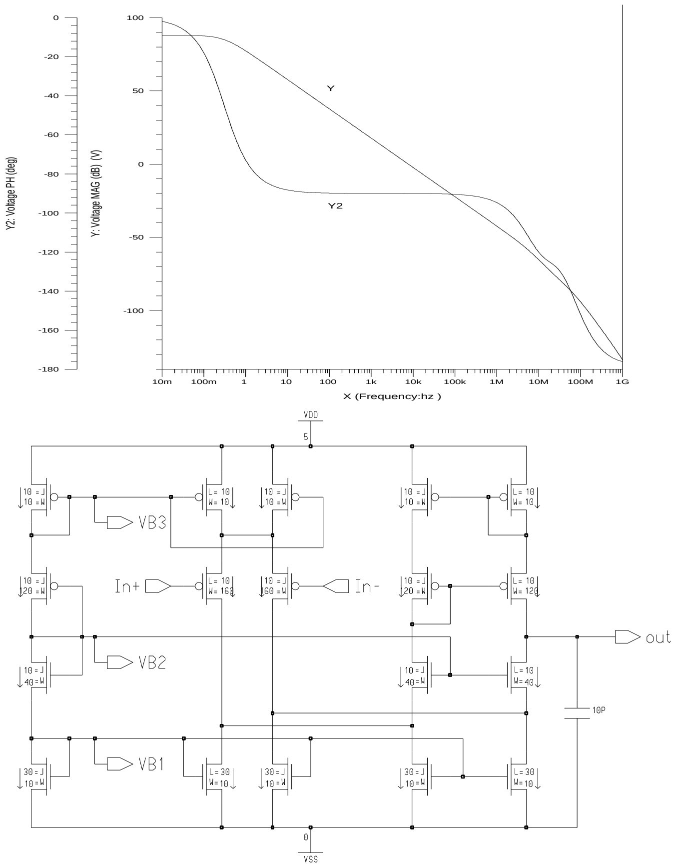

Figure 4. Op-amp with minimum size PMOS.

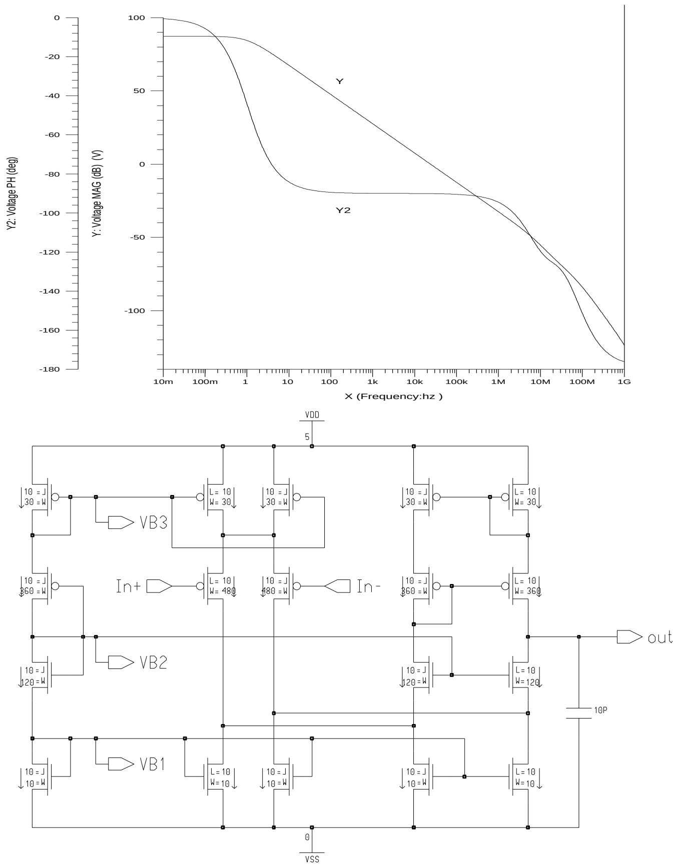

Figure 5. Op-amp with minimum size NMOS.

area used by $N3$ and $P3$. This would not have been possible without the insight provided by the gain formula for the constrained design.

3.2. Optimizing area under a slew-rate constraint

A side effect of using long transistors for $N1$ and $P1$ for minimizing the area is a simultaneous reduction in current consumption. For some low power applications the reduced current is beneficial but many times the lower bound on current consumption is determined by the required slew rate: $SR = 2I/C_L$ [7]. If the current obtained by optimizing the area is smaller than required by the slew rate we can increase the current from the optimal value or we can use an output stage. In this section we consider the first alternative, the use of an output stage being discussed later.

For increasing the current while keeping the ratio x constant we can simply use table 2 and multiply all the widths by a given constant and then simplify the ratios W/L to make sure that either $W = w$ or $L = l$. If we multiply by 2 we obtain the case where $P1$ is minimum size and if we multiply by 6 we obtain the case where $N1$ is minimum size (see table 3). The schematics and Bode plots for the two cases with larger current are shown in figures 4 and 5. Again it should be noted how easy it is to synthesize op-amps with different performance using only simple calculations. The layouts for all these cases is very similar as should be the case for a "firm" component.

3.3. Maximizing the slew-rate for minimum area

A very different result is obtained if the gain is no longer the objective function. In order to maximize the current (i.e. slew-rate $SR = 2I/C_L$) we need to maximize the formula:

$$I = \frac{1}{2}\mu_n \cdot C_{ox} \cdot W/L \cdot (V/2 - 2V_{th})^2 \cdot \frac{x}{(1+\sqrt{x})^2}$$

Differentiating with respect to x we obtain that the current is maximized for $x = 1$. This does not satisfy the condition $x \geq m$ which was used for table 2 so we need to recompute the sizes for minimum area as in table 4.

3.4. Output stage with the symmetry-based method

Finally, an output stage can be designed using the Symmetry-based rules. For example an op-amp with a Symmetry-based source follower output stage is shown in figure 6. As can be seen from the layout in figure 7 the new circuit has now 7 transistor columns that preserve the robustness to parameter variations and the ease of layout.

Table 3. Transistor sizes for higher slew-rate.

dimension	min PMOS	min NMOS
W_{n1}	10	10
L_{n1}	30	10
W_{n3}	40	120
L_{n3}	10	10
W_{p1}	120	360
L_{p1}	10	10
W_{p3}	10	30
L_{p3}	10	10
W_{p6}	160	480
L_{p6}	10	10

Table 4. Sizes for maximum slew-rate.

dimension	value	numeric
W_{n1}	w	10
L_{n1}	$l\sqrt{m}$	17
W_{n3}	w	10
L_{n3}	$l\sqrt{m}$	17
W_{p1}	$w\sqrt{m}$	17
L_{p1}	l	10
W_{p3}	$w\sqrt{m}$	17
L_{p3}	l	10
W_{p6}	$2w\sqrt{m}$	34
L_{p6}	l	10

4. Conclusions

We have presented a design methodology for op-amps as "firm" Virtual Components for Systems-on-Chip. The resulting design is robust to process variation and to process migration, and the resulting virtual components are easy to generate by computer, have a very regular layout, and can be easily scaled for different performance levels. The method can be extended to other types of circuits in order to create a library of virtual components.

Acknowledgements

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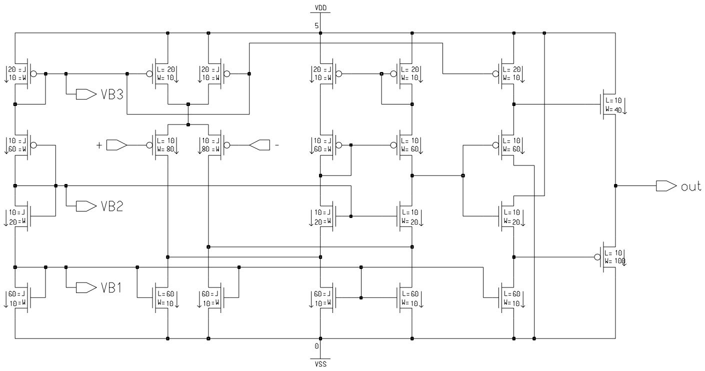

Figure 6. Op-amp with output stage.

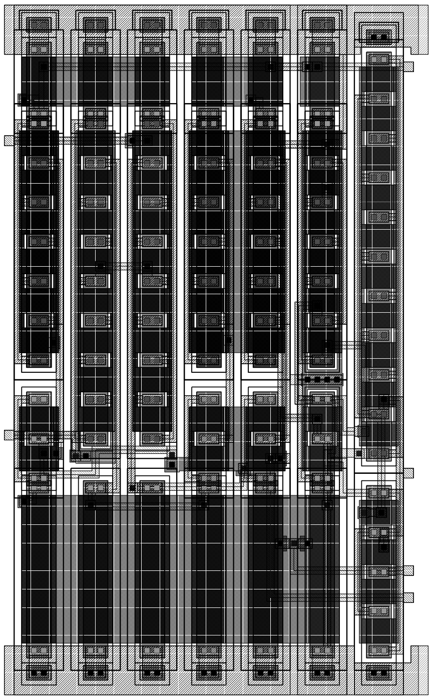

Figure 7. Layout for op-amp with output stage.

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