Ti Quadlevel Resist Process for the Fabrication of Nb SIS Junctions

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Abstract—We have fabricated high quality Nb/Al-oxide/Nb Superconductor-Insulator-Superconductor (SIS) junctions using a Ti-based quadlevel resist process. The quadlevel materials have been carefully chosen to optimize the fluorine-based anisotropic reactive ion etching of Nb and subsequent insulation coverage of the junctions in a self-aligned process. This SIS fabrication process enables excellent control of junction size and is also compatible with Au overlayer junction and junction anodization approaches.

Index Terms—Nb, Quadlevel, Resist, Superconductor, SIS

I. INTRODUCTION

For millimeter and sub-millimeter wavelength SIS mixers, the process for fabricating the actual junctions is typically the most complicated and demanding of the entire wafer circuitry. As designs become more complex, and as the number of elements on a given wafer decreases, the control of junction size and insulation thickness across the wafer becomes even more critical. Since junction sizes are typically smaller than 3µm in diameter, machine-aligned techniques are typically not useful for separate registration of the junction and the insulation patterns [1]. The allowable junction fabrication techniques therefore can generally be classified into planarization/etch-back [2] and self-aligned processes [3-7].

For the planarization and etch-back technique, since the junction etch is performed in a process separate from the insulation definition, the junction can be defined with a thin, high resolution resist and the wafer thoroughly cleaned before deposition of the junction insulation. Challenges in the process include successful endpoint detection of the Nb counter electrode during the insulation etch back and control of the final thickness and uniformity of the junction insulation layer.

The advantages of the self-aligned technique, in addition to not requiring the necessary etch-back equipment, include more design flexibility in the choice of a range of junction insulation thickness, and typically better control of uniformity of the final thickness of the insulation layer. The greatest challenge in this process typically centers on the development of a working junction resist scheme that permits both precise definition and control of junction area, and also permits liftoff of a junction insulation layer that will protect the base electrode from the subsequent wiring/interconnection layer.

We developed the first trilevel resist scheme for a self-aligned SIS junction insulation process [8,9]. Trilevel resists typically are composed of a thicker bottom organic planarization layer, a thinner inorganic ‘barrier’ and a top imaging layer of photoresist. They are attractive for SIS junction resist processes for a number of reasons. Since the imaging resist is only required to serve as an etch mask for the thin inorganic barrier layer, a thin high resolution imaging resist can be used. If anisotropic etches are used to remove the trilevel barrier and planarization layers, then high resolution features can be obtained in a relatively thick trilevel structure for improved liftoff. The inorganic trilevel barrier layer provides the added benefit of a durable ‘top’ to the resist structure. This permits the flexibility of using argon ion etching or lateral shrinking of the organic layer with an O₂ plasma without degradation of the resist profile and height.

In our original scheme, a 1-2µm polyimide layer and a 140nm thick SiO₂ layer were used for the trilevel planarization and barrier layers, respectively. The choice of these materials was less than optimum, though in general junctions with excellent electrical qualities were obtained. A relatively thick SiO₂ barrier layer was required since the CF₄-based chemistry, used to etch the Nb junction counter electrode, also removed SiO₂ at a relatively high etch rate. With an SiO₂ layer of this thickness, a thicker and lower resolution imaging resist in turn was needed. The O₂ planarization etch resulted in considerable debris on the wafer surface, which was only partially removed in a subsequent hydrofluoric acid-based wet etch. The CF₄-based Nb junction RIE chemistry etched the Nb junction electrode isotropically, with any over etching resulting in increased undercutting. This unpredictable loss of junction linewidth required an O₂ plasma ‘shrink’ of the planarization layer after the junction etch to insure that the insulation layer (SiO) fully covered the sidewalls of the Nb junction button. This shrink process was difficult to control due to fluorine hardening of the polyimide sidewalls. The unpredictability of the junction size across the wafer also reduced the yield of usable mixer elements.

We have since made numerous changes to this technique, transforming it into a versatile quadlevel resist process for fabricating high quality Nb/Al-oxide/Nb junctions, with excellent control of junction size.
II. EXPERIMENTAL

The equipment used to deposit our Nb/Al-oxide/Nb trilayer films has been described previously [10]. This system has since been modified; it is pumped with a 900 L/s turbo pump, the sputtering sources have been replaced with K.J. Lesker 3 inch magnetron guns, the Meissner trap has been removed, and an Au sputtering source has been added to the system for Au over-layer trilayer processes. All trilayer films have expected stress of less than 1.5 x 10^4 dynes/cm^2.

The equipment used to deposit the multilevel resist barrier layer is a multi-target sputtering system with a focused five gun geometry. The spacing between the target of the US Inc. gun and wafer is approximately 14 cm. The substrate platter rotates on axis directly above the gun focus. The base pressure of this system is 1 x 10^-9 Pa.

A Semigroup Inc. RIE was used for all multilevel resist structure etching. The water-cooled, RF-powered stainless steel platter area is ~730 cm^2 with an electrode spacing of 4.5 cm. The base pressure of this system is 1 x 10^-4 Pa.

One of the main deficiencies of our trilevel resist technique has been the lack of a trilevel barrier material that takes full advantage of the potential capabilities of the process. A wet etch defined, sputtered Cr barrier material, compatible for use with a thin, high resolution resist, was used successfully. However, it was difficult to control junction sizes smaller than 3 µm and the wet etch would often completely undercut Cr features for junctions smaller than 2 µm. JPL has developed a Cr trilevel resist process where extremely small barrier features were defined by Ebeam-liftoff [11]; however, we do not have daily access to an Ebeam tool.

More recently, we have implemented a trilevel resist with a Nb-based trilevel barrier, as shown in Fig. 1. The trilevel Nb can be RIE etched anisotropically with a thin imaging resist such that trilevel resist features with small linewidths can be accurately defined. This trilevel Nb, however, is also etched in the subsequent Nb junction etch. Even with a trilevel Nb layer 2 to 3 times thicker than the counter electrode, the trilevel Nb is often completely removed. As is shown in Fig. 1, the trilevel Nb is almost completely removed; a rim of back-sputtered material from the planarization etch marks the previous perimeter of the trilevel Nb button. For the case of complete removal of the trilevel Nb, a large source of debris is introduced from both the etching of the polyimide surface and from the fragments of the back-sputtered rim.

To solve this problem, we have developed a Ti-based barrier process. Titanium was chosen after it was realized that Ti could be very anisotropically patterned with an F12 (CCl₂F₂) RIE etch. Ti is etched in our present SF₆-based Nb RIE process, but at almost a factor of four less than Nb. The Ti RIE etch conditions are F12 11sccm, CF₄ 4sccm and O₂ 2sccm at 4 Pa and 120 W. Using the negative NFR resist [12] for the imaging resist, one can over etch the 100nm thick Ti layer by 40% with no loss of linewidth.

Another significant drawback to our previous SIS junction trilevel resist process is the lack of anisotropy in the Nb junction etch. While the earlier etch chemistry of CF₄ plus O₂ resulted in significant undercutting, a change to an SF₆ plus N₂ etch [13] gave much improved anisotropy. Our earlier SIS mixer designs permitted the use of a ‘light’ anodization and/or a relatively thick (>400nm) junction insulation layer to insure full base electrode insulation and protection from the subsequent wiring/interconnection layer. Most of our present designs, however, do not permit junction anodization and require an insulation thickness on the order of 200nm. Because of this, much of our SIS junction fabrication is based on the JPL Au overlayer technique [14] where a ~30nm layer of Au is left on top of the junction electrode. This Au cap permits a Nb wiring process without any in-situ ion cleaning (avoiding physical disturbance of the junction insulation) due to the lack of Au native oxide. This technique permits the use of relatively thin insulation layers (~150nm) to successfully insulate the base electrode from the subsequent Nb wiring-interconnection layer.

The incorporation of this Au overlayer technique into our process presented a number of difficulties. The most significant was the loss of anisotropy in our SF₆ plus N₂ Nb junction etch. The presence of a Cr-Au ‘button’ on top of the Nb film surprisingly changes either the chemistry of the etch or the local bias conditions. The addition of CHF₃ to the RIE chemistry partially improved the anisotropy of the Au-overlayer Nb etch. We have discovered; however, that the NFR chemistry can dramatically improve the anisotropy of fluorine-based Nb etching. The resist is based on a novolak resin with a melamine derivative and thinned with methyl-3-methoxy propionate. We first examined NFR in a single-resist system for a Au overlayer process, using the resist as a mask to first wet etch the Cr-Au overlayer and then to RIE etch the Nb counter electrode junction button. The anisotropy of this single resist was excellent, as is shown in Fig. 2. However, the lack of a suitable NFR resist stripper that is compatible with the Nb/Al-oxide/Nb material system (the resist is designed for ion implantation applications) prevents the application of this single layer NFR resist to a self-aligned SIS junction technology.

![Fig. 1. A Nb-based trilevel resist feature used to etch a Nb junction button from a Nb/Al-oxide/Nb trilayer film. Note that the trilevel Nb is almost completely removed.](image-url)
The previously-used, polyimide trilevel planarization layer was therefore modified to take advantage of the NFR-enhanced anisotropy of the Nb RIE. We developed a quadlevel resist structure where sequential layers of 200nm thick NFR and 200nm thick polyimide layers are spun to form a bi-layer planarization layer. The manufacturer engineers the NFR resist for enhanced adhesion to partially cured polyimide layers. An SEM image of the Ti-based quadlevel resist after RIE of the planarization bilayer is shown in Fig. 3. An O$_2$ plus CHF$_3$ RIE etch (15sccm O$_2$, 15sccm CHF$_3$, ~0.7Pa, 700V bias) is used to etch the NFR and polyimide. The CHF$_3$ is added to our O$_2$ planarization etch to give straighter side walls. The resulting profile is typically slightly hour-glass in shape, with the bottom ‘foot’ of the NFR having a diameter just less than the Ti etch mask. The etch is performed under a 150mm crystal-grade polystyrene petri dish supported by three Teflon posts ~50mm above the wafer. The wafer is placed in a second petri dish on top of a quartz platter. The bottom dish reduces debris from backspattering and the top platter protects against debris generated from the upper platter.

The effect of the NFR is excellent, with anisotropic fluorine-based RIE etching of the counter electrode Nb. As is shown in Fig. 4, the NFR resist has not only enhanced the anisotropy of the Nb RIE etch, but also serves as an excellent mask for the Au wet etch. Our HG-800 Cr-Au wet etch is composed of I 10g, INH$_4$ 40g, DI water 900ml, and ethanol 1100ml. The etchant requires approximately 25 seconds to completely remove 30nm of Cr-Au after a short O$_2$ plasma clean. In contrast to the significant undercutting obtained with the polyimide etch mask of the trilevel resist, the NFR chemistry results in a Au profile that is flush with, or slightly protruding beyond the sidewalls of the NFR planarization layer. We are therefore surprisingly able to use this wet etch with the quadlevel resist to define Cr-Au overlayers as small as 0.5μm.

In our new fabrication process, the perimeter of the Nb junction button is defined by the largest feature above it. This is shown clearly in Fig. 5, where an extended O$_2$ planarization etch was performed to yield a planarization layer perimeter that significantly undercuts the Ti barrier layer. While the Au wet etch results in a Au profile in line with the NFR perimeter, the subsequent Nb RIE etch follows the Ti perimeter and not the NFR. This result implies that the junction size is determined by the Ti mask and not by the profile of some other, less accurately controlled resist feature. It is also interesting to note that a switch in the order of the planarization bi-layer changes the entire dynamics of the etching process. Surprisingly, the benefit of the NFR chemistry on the Au-overlayer Nb RIE process is lost if the NFR is not directly in contact with the overlayer Cr-Au.

After junction insulation, the quadlevel resist is lifted off in a two-step process. The polyimide and overlapping
We have developed a new Ti-based quadlevel junction resist technique for the insulation of Nb/Al-Oxide/Nb SIS junctions. This technique allows accurate and uniform RIE definition of the upper Ti ‘barrier’ layer with a thin, high resolution imaging resist. The planarization material of this quadlevel resist is composed of an upper polyimide layer and a lower NFR resist. The NFR planarization layer is an excellent mask for our wet etch of the Cr-Au overlayer. The quadlevel resist technique has been used in a variety of junction fabrication processes. For mixer designs requiring thick junction insulation layers, the typically 400nm thick planarization bi-layer can easily be increased to enable liftoff. This quadlevel process is also used to fabricate mixers that require junction anodization [15]. For this process, the wafer should be hot plate baked at 120°C for 5 minutes prior to anodization to improve adhesion of the planarization NFR to the junction electrode and then cleaned briefly in an oxygen plasma to insure complete wetting of the wafer by the anodization fluid. Though it did not seem to affect the junction sealing capabilities of the anodization process, some of the trilevel Ti barrier etch mask buttons were somehow also anodized in the process.

III. SUMMARY

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REFERENCES


