Hot-Electron Bolometers on Ultra-thin Silicon Chips with Beam Leads for a 585GHz Receiver

A Dissertation Presented to the Graduate Faculty
of the School of Engineering and Applied Science of the University of Virginia

In Partial Fulfillment
of the Requirements of the Degree
Doctor of Philosophy in Electrical Engineering

by

Robert Bruce Bass III

May 2004
© Copyright by

Robert Bass

All Rights Reserved

May 2004
Hot-Electron Bolometers on Beam Lead Chips for a 585GHz Receiver

A Dissertation Presented to the Graduate Faculty
of the School of Engineering and Applied Science of the University of Virginia
In Partial Fulfillment of the Requirements of the Degree
Doctor of Philosophy in Electrical Engineering

by

Robert Bruce Bass III

May 2004
For Sarah
Approval Sheet

This Dissertation is submitted in partial fulfillment of the Requirements for the Degree of Doctor of Philosophy in Electrical Engineering

Author

The Dissertation has been read and approved by the Examining Committee:

[Signatures]

Accepted for the School of Engineering and Applied Science:

Dean
School of Engineering and Applied Science

May 2004
Abstract

Interest in observing astronomical phenomena within the terahertz frequency spectrum has driven demand for extremely sensitive heterodyne receivers. Radio astronomers use observatories such as the 12 meter Kitt Peak telescope in Arizona and the James Clerk Maxwell telescope atop Mauna Kea in Hawaii to probe molecules and dust in interstellar clouds, the dynamics of star formation, proto-planetary discs, and other astronomical phenomena. Additional terahertz applications include atmospheric spectroscopy, remote sensing, bio-particle detection, and terahertz medical imaging.

Novel devices for heterodyne mixing, such as ultra-thin silicon chips and hot-electron bolometers (HEBs), will extend the experimental capabilities of receivers into the terahertz frequency domain.

We developed and integrated several submillimeter-wave technologies that improve the design and assembly of terahertz receivers. The first of these, ultra-thin silicon chips with gold beam leads, is an innovative approach for mounting non-linear circuit elements and other microwave circuit structures within a terahertz waveguide receiver. These chips will also facilitate the development of large format arrays of terahertz receivers, which integrate multiple receivers onto a single micromachined array frame. The second involves the fabrication of phonon-cooled and diffusion-cooled HEBs, which have device dimensions of less than a quarter-micron. These new bolometer fabrication processes rely on electron-beam lithography to define sub-micron device dimensions. This dissertation demonstrates the functionality of the ultra-thin silicon chips as well as the hot-electron bolometers, and sets the stage for radio frequency testing of these technologies in a 585GHz receiver.
Acknowledgements

I would like to begin by expressing my genuine gratitude to my advisor, Dr. Arthur Lichtenberger, who opened the first door for me more than once. The freedom he provided for me to err and succeed on my own has been invaluable. I could imagine neither a better student/advisor relationship, nor a more ideal research environment.

Research and teaching go hand-in-hand in engineering academics, and it is difficult to juggle both of these aspects well. I sincerely appreciate those professors who have made teaching the defining goal of their academic careers, especially Dr. Robert Weikle, Dr. Lloyd Harriott, and Dr. Steven Wilson. I admire their dedication to academics and the teaching process, as well as their devotion to the development of their students, in both the classroom and the laboratory.

I could not have gotten through this work without the contributions and support generously offered over the years by the staff and research scientists of the Electrical Engineering and Physics laboratories, especially Jian-Zhong Zhang, Bill Bishop, Joe Beatrice, Acar Isin, and Alex Lobo. This dissertation would not have been possible without them.

I want to acknowledge the many graduate students whose company and conversation was often helpful, other times amusing, and frequently both. From the past and present, these include SIS group members Bowe Ellis, Aaron Datesman, and Jon Schultz; FIR folks Nagini Paravastu, Haiyong Xu, and Qun Xiao; and former officemates Matt Hunt, Gerhard Schoenthal, and Will Clark.

During my years at the University, I have run across many strange and wonderful people. A list of all these folks would be exhaustive and, most likely, incomplete. So,
rather than listing them all individually, I would simply like to thank the whole lot for just being around during the whole journey.

And finally, I cannot neglect to mention the members of my family, whom I cherish above all else. I offer my sincerest thanks to my parents, Margaret and Robert Bass, for their boundless support and guidance, and without whom I could never have completed graduate school, let alone even take the first steps. They have provided the means and direction for a wonderful life. My brother John, too, has always been there for me, and our uniquely strange relationship will always remind me of the view through the looking glass. I save my greatest thanks to my very best friend Sarah, with whom I stand beside, now and forever.
## Table of Contents

Approval Sheet .................................................................................................................... v
Abstract ................................................................................................................................ vi
Acknowledgements ........................................................................................................... vii
Table of Contents ............................................................................................................... x
List of Figures ................................................................................................................... xii
List of Tables .................................................................................................................... xiv
List of Symbols ............................................................................................................... xv
Chapter 1 Introduction ........................................................................................................ 1
  1.1 Heterodyne Mixing .................................................................................................. 4
  1.2 Technology Limitations at THz Frequencies ........................................................... 6
    1.2.1 Submillimeter Circuit Limitations .................................................................... 7
    1.2.2 Limitations of Receiver Assembly .................................................................... 8
  1.3 References ............................................................................................................... 10
Chapter 2 State of the Art ................................................................................................ 14
  2.1 Submillimeter-wave Circuit Mounting Techniques ............................................... 14
  2.2 Hot-Electron Bolometers ....................................................................................... 17
    2.2.2 Phonon-Cooled Hot-Electron Bolometer Theory ............................................ 18
    2.2.2 Diffusion-Cooled Hot-Electron Bolometer Theory ......................................... 20
    2.2.3 RF Operation .................................................................................................... 21
  2.3 Nanometer-Scale Fabrication at UVa .................................................................... 22
    2.3.1 Direct FIB Fabrication .................................................................................... 23
    2.3.2 Microcontact Printing ..................................................................................... 23
  2.4 Electron-beam Lithography ................................................................................... 25
    2.4.1 SEM Basics ..................................................................................................... 26
    2.4.2 Resolution Limits of EBL ............................................................................... 26
    2.4.3 The Nanometer Pattern Generation System (NPGS)....................................... 27
  2.5 A Review of EBL-Fabrication Methods for HEBs................................................ 28
    2.5.1 The JPL Process .............................................................................................. 29
    2.5.2 The SRON Processes ...................................................................................... 30
  2.6 References ............................................................................................................... 34
Chapter 3 Design of the 585GHz Receiver ....................................................................... 39
  3.1 Receiver Design ...................................................................................................... 41
    3.1.1 Low-pass Filter ................................................................................................ 41
    3.1.2 Bowtie Antenna Design ................................................................................... 46
    3.1.3 SOI LPF Microstrip Channel ........................................................................... 49
    3.1.4 Reduced-Height Waveguide and Backshort .................................................... 51
    3.1.5 Diagonal Feedhorn ........................................................................................... 53
  3.2 HFSS Simulations ................................................................................................... 53
    3.2.1 585 Upright Receiver Design ........................................................................... 54
    3.2.2 90° 585 Design ................................................................................................ 57
    3.2.3 Spatial Variations in Chip Location and Backshort Length ................................ 63
    3.2.4 Substituting Quartz for Silicon ........................................................................ 64
  3.3 Block Design ........................................................................................................... 66
### Table of Contents

3.4 Mask Design ........................................................................................................... 71
3.5 References ............................................................................................................... 73

**Chapter 4 Fabrication of Ultra-Thin Silicon Chips with Beam Leads**

4.1 Fabrication ............................................................................................................. 80
  4.1.1 Beam lead fabrication ...................................................................................... 82
  4.1.2 Silicon thinning ............................................................................................... 83
  4.1.3 Chip Definition ............................................................................................... 86
4.2 Discussion ............................................................................................................... 91
4.3 Conclusion .............................................................................................................. 93
4.4 References ............................................................................................................. 94

**Chapter 5 Fabrication of Diffusion-Cooled Hot-Electron Bolometers**

5.1 d-HEB Fabrication ............................................................................................... 98
  5.1.1 HEB Niobium Deposition .............................................................................. 100
  5.1.2 Cooling Pad Definition .................................................................................. 101
  5.1.3 Niobium Mask Definition .............................................................................. 106
  5.1.4 Microbridge Etching ...................................................................................... 112
  5.1.4 Passivation ..................................................................................................... 113
5.2 Results ................................................................................................................... 114
5.3 References ............................................................................................................. 116

**Chapter 6 Fabrication of Phonon-Cooled Hot-Electron Bolometers**

6.1 p-HEB Fabrication ............................................................................................... 120
  6.1.1 NbN Film Deposition .................................................................................... 121
  6.1.2 Bridge Length Definition ............................................................................... 122
  6.1.3 Bridge Width Definition ................................................................................ 124
  6.1.4 NbN Etching .................................................................................................. 125
6.2 Results ................................................................................................................... 126
6.3 References ............................................................................................................. 132

**Chapter 7 Results and Conclusions**

7.1 Cryogenic Device Testing .................................................................................... 134
7.2 Receiver Assembly, DC Testing and Results ....................................................... 138
  7.2.1 Receiver Assembly ........................................................................................ 140
  7.2.2 DC Testing ..................................................................................................... 141
  7.2.3 Disassembly ................................................................................................... 144
7.3 Future Work .......................................................................................................... 146
7.4 Conclusion ............................................................................................................ 151
7.5 References ............................................................................................................. 158

**Appendix 1 Fabrication of Quartz Chips with Gold Beam Leads**

A1.1 Beam Lead Fabrication ...................................................................................... 162
  A1.1.1 Trench Definition ....................................................................................... 163
  A1.1.2 Epoxy Planarization ................................................................................... 165
  A1.1.3 Beam lead Fabrication ............................................................................... 169
A1.2 Planarization Results ........................................................................................ 173
A1.3 Conclusion ......................................................................................................... 175
A1.4 References ......................................................................................................... 176

**Appendix 2 Equipment List**

A2.1 Chemicals ........................................................................................................... 178
A2.1.1 Cryogenic Liquids ................................................................. 178
A2.1.2 Developers .................................................................................. 178
A2.1.3 Photo/E-beam Resists ............................................................... 178
A2.1.4 Reactive Ion Etching Gases ......................................................... 179
A2.1.5 Solvents ......................................................................................... 179
A2.2 Computer Programs ....................................................................... 179
A2.3 Equipment ....................................................................................... 179
A2.4 Evaporator/Sputter Metals .............................................................. 180
A2.5 Other Parts ....................................................................................... 180
A2.6 Wafers ............................................................................................ 180
Appendix 3 Publications .......................................................................... 181
List of Figures

Inside Cover: An ultra-thin silicon chip featuring an HEB and beam leads.

2.1 Cross-section diagram of chips in microstrip channels.

3.1 The 600GHz SMA receiver and the 585GHz Receiver.
3.2 A diagram of a microstrip line.
3.3 A diagram of the first two section of a low-pass filter.
3.4 Plot of $Z_{IN}$ versus the number of filter elements.
3.5 Flag length and taper angle of a bowtie antenna.
3.6 Bowtie impedance versus flag length.
3.7 Bowtie impedance versus taper angle.
3.8 Cross-section along the width of a microstrip channel.
3.9 HFSS wire frame model of the upright 585 design.
3.10 HFSS wire frame model of the 90° 585 design.
3.11 Magnitude of $s_{31}$ plotted versus frequency for the upright design and 90° design.
3.12 Magnitude of $s_{31}$ versus frequency.
3.13 Magnitude of $s_{21}$ versus frequency.
3.14 Magnitude of $s_{22}$ versus frequency.
3.15 Smith chart of $s_{11}$.
3.16 Dimension offset Smith charts of $s_{11}$.
3.17 Smith charts of $s_{11}$ for quartz chips.
3.18 CAD layout of the assembled receiver block.
3.19 CAD drawings of the top half of the receiver block.
3.20 CAD drawings of the bottom half of the receiver block.
3.21 CAD close-up of the mating face of the bottom half of the receiver block.
3.22 CAD cross-section along the length of the microstrip channel.
3.23 CAD cross-section along the length of the reduced-height waveguide.
3.24 Base mask CAD drawing.
3.25 Plating mask CAD drawing.
3.26 Chip extents CAD drawing.
3.27 Mask composite.

4.1 Process diagram for ultra-thin silicon chips with beam leads.
4.2 CAD drawing of an etching jig.
4.3 Photoresist backside-patterned on ultra-thin silicon.
4.4 Two ultra-thin silicon chips after RIE.
4.5 Graph of etch time versus silicon thickness.
4.6 A completed ultra-thin silicon chip with beam leads.
4.7 Two SEM micrographs of completed silicon chips.
4.8 An ultra-thin silicon chip with beam leads in a microstrip channel.

5.1 A schematic diagram of the d-HEB fabrication process.
5.2 A schematic diagram of the bilayer resist process.
5.3 A histogram comparing the pattern deviation of two writing processes.
5.4 Cooling pads after lift-off.
5.5 A chart relating actual bridge length to CAD pattern spacing.
5.6 A chart of pattern deviation as a function of CAD pattern width.
5.7 A scatter plot showing linewidth as a function of line dose.
5.8 A chart showing average linewidths versus line dose, and a curve fit.
5.9 A microbridge etch mask spanning the cooling pads of a d-HEB.
5.10 Average microbridge width as a function of line dose.
5.11 A completed HEB on a silicon substrate.
5.12 Resistance versus temperature measurements of a d-HEB fabricated on silicon.

6.1 A schematic diagram of the p-HEB fabrication process.
6.2 Resistance versus temperature plot of a NbN thin film.
6.3 Cooling pads of a p-HEB.
6.4 SiO₃ mask above a p-HEB junction.
6.5 Resistance versus temperature plot of a p-HEB.

7.1 Current versus voltage plot of a p-HEB.
7.2 Resistance versus temperature plot of a p-HEB.
7.3 Mating face of the 585GHz receiver block.
7.4 An ultra-thin silicon chip within the microstrip channel of the 585GHz receiver.
7.5 Current versus voltage plot of a p-HEB mounted inside the 585GHz receiver.
7.6 A chip in a microstrip channel after disassembling the block halves.
7.7 Mating face of the 585GHz receiver block with indentations from beam leads.
7.8 HFSS model of a 16-element HEB imaging array.
7.9 SEM micrograph of an integrated ultra-thin silicon chip.
7.10 SEM micrograph of an integrated ultra-thin silicon chip.

A1.1 Outline of the quartz beam lead process.
A1.2 Quartz mesas surrounded by 150µm deep trenches.
A1.3 Diced quartz trenches in cross-section.
A1.4 The epoxy-pouring jig.
A1.5 Planarized trenches in cross-section.
A1.6 Quartz mesas surrounded by planarized trenches.
A1.7 1.8µm thick gold beam leads on a quartz substrate.
A1.8 A planarized quartz substrate and a map of approximate scan locations.
A1.9 Epoxy planarization profiles.
A1.10 A completed quartz chip with beam leads and RF circuitry.
List of Tables

3.1 Physical line length as a function of characteristic impedance.
3.2 $Z_{\text{high}}$ and $Z_{\text{low}}$ characteristic impedances for low-pass filter segments.
3.3 Flag length and taper angle of the 585GHz designs and the SMA design.
3.4 Dimensions for various microstrip waveguide channels simulated using HFSS.
3.5 Measurements of $s_{11}$ as a function of backshort length.
3.6 Design parameters and calculated impedance values for silicon chips at 585GHz.
3.7 Design parameters and calculated impedance values for the 90° receiver design.
3.8 Design parameters and calculated impedance values for quartz chips.

4.1 A list of beam lead batches with specifications.

5.1 Resistance data from a batch of d-HEBs.

6.1 Relationship between annealing time and temperature to transition temperature.
6.2 Relationship between annealing time and temperature to sheet resistance.
List of Symbols

A - Ampere
b - Rod width, beam width
C - Degree Celsius
C - Capacitance
Ce - Electron specific heat capacity
Cph - Lattice (phonon) specific heat capacity
c - Speed of light in a vacuum
D - Electron diffusion constant
DC - Direct current
d - Thickness, rod thickness
dB - Decibels
E - Electric field
E - Modulus of elasticity (Young’s modulus)
Fr - Load at failure
f - Frequency
G - Thermal conductivity (length independent)
H - Microstrip channel height
H - Magnetic field
Hz - Hertz
I - Current
Ic - Critical current of a superconductor
IF - Intermediate frequency
i - The imaginary number ‘i’
J - Joules
jc - Critical current density of a superconductor
K - Degree Kelvin
K - Thermal conductivity
kg - Kilogram
L - Length
LO - Local oscillator frequency
l - Physical line length
l_e - Electron diffusion length
l_e-ph - Electron-phonon interaction length
mol - Mole
m - Meter
nm - Nanometer
P - Power
Q (dot) - Heat flow
R - Resistance
Rn - Normal-state resistance
RF - Radio frequency
S - Voltage sensitivity
s - S-parameter
T - Temperature
Tc - Critical temperature of a superconductor
t - Time
Ur - Resilience
V - Volt
v - Velocity of sound
W - Watts
W - Width
X - Reactance
Z - Impedance
α - Phonon coefficient of transmission
ΔT - R-T curve transition width
ΔT - Temperature difference
Γ - Reflection Coefficient
ε0 - Permeability of free space
εr - Dielectric constant
Θ - Electrical line length
λ - Wavelength
μm - Micron
π - Pi
ρ - Resistivity
σmr - Modulus of rupture
σy - Yield strength
τ - Thermal relaxation time
τES - Phonon escape time
τe-e - Electron-electron interaction time
τph - Electron-Phonon interaction time
τth - Thermal relaxation time
Ω - Ohm
Ω/□ - Sheet resistance. Ohms per square
ω - Angular frequency (2πf)
Chapter 1

Introduction

Interest in observing astronomical phenomena within the terahertz frequency spectrum (1mm to 100μm wavelengths) has driven demand for extremely sensitive heterodyne receivers. Traditionally, the radio astronomy community uses niobium-based SIS (superconducting-insulating-superconducting) tunnel junctions for observations below 700GHz. Present-day observatories, such as the 12-meter Kitt Peak telescope in Arizona and the James Clerk Maxwell telescope atop Mauna Kea in Hawaii, use low-noise SIS mixers fabricated by our research group. Radio astronomers use these observatories to probe molecules and dust in interstellar clouds, the dynamics of star formation, proto-planetary discs, and other astronomical phenomena [1]. THz devices are not limited to radio astronomy applications; other terahertz applications include atmospheric spectroscopy, remote sensing, bio-particle detection, and terahertz imaging [2-4]. Novel technologies, such as hot-electron bolometers (HEBs) for heterodyne mixing and ultra-thin silicon chips, will extend the experimental capabilities of receivers into the THz frequency domain.

The SIS research group within the Department of Electrical and Computer Engineering is a leader in the fabrication of superconducting heterodyne mixer circuits. The bulk of our work centers on the development of niobium-based SIS mixers fabricated atop quartz substrates. These are single-element receivers, which rely on waveguides to couple RF radiation from a feedhorn antenna to the mixer chip [5,6]. Single-element
waveguide receivers are standard for SIS- and HEB-based receivers, with the exception of a few arrayed waveguide receivers consisting of SIS mixers [7,8].

Our research group, in cooperation with researchers at the University of Arizona and the California Institute of Technology, has also made progress towards integrating HEB mixers atop silicon nitride membranes as another approach for assembling receiver arrays [9]. Integrated arrays offer the benefits of rapid assembly and dense receiver integration since all of the mixers are fabricated atop a single chip. However, all of the devices on the array chip must have similar characteristics and cannot fail. In addition, the silicon nitride membranes must be extremely thin, around 1μm or so, at which point the membranes are extremely brittle and difficult to handle. Failure of any one of the mixing devices or membranes on a chip would lead to a loss in pixel density, jeopardizing receiver performance and possibly requiring the replacement of the entire mixer array chip.

I realized these problems could be circumvented if each mixing element of an array was fabricated atop a single, smaller chip that could be placed within an array frame. By contacting these ultra-thin chips to the array frame via beam leads, the array could be quickly assembled with pre-tested devices, and these devices could later be individually removed without disturbing the other elements within the array frame [10]. In addition, ultra-thin silicon chips could be used in single-element metal waveguide receivers, greatly reducing the amount of dielectric within a waveguide channel and facilitating rapid prototyping and device replacement.

Ultra-thin chips with beam leads would be a powerful technology for THz mixers if several considerations could be met. First, the technology would have to be compatible
with SIS and HEB fabrication processes. Second, the chips would need to be approximately 1μm to 10μm thick, and must be robust enough to survive receiver assembly and repeated thermal cycling down to cryogenic temperatures. And finally, because these chips must be incredibly thin, they would have to be integrated with beam leads in order to mount them within THz receiver blocks or array frames.

My fabrication process utilizes silicon-on-insulator (SOI) substrates integrated with gold beam leads to achieve ultra-thin silicon chips, and is a unique idea that we first implemented and published in 2003 [11]. Given our earlier work on beam leads for quartz-based millimeter-wave mixers, I realized that the solution to the requirements mentioned above lay in the integration of beam lead technology with SOI substrates [12,13]. Ultra-thin chips could be defined from the device layer of an SOI substrate while the handle layer of silicon would provide mechanical rigidity during preceding processing steps.

In this dissertation, I present the design, assembly and DC testing of a 585GHz heterodyne receiver. I designed the receiver specifically to demonstrate the feasibility of ultra-thin silicon chips with beam leads in THz receiver structures. The receiver features a hot-electron bolometer and RF circuitry fabricated atop an ultra-thin silicon chip. The development of these technologies was not straightforward. Before I initiated the work presented in this dissertation, our research group had no experience with beam lead devices, electron-beam lithography, or ultra-thin silicon substrates. Our experience with diffusion-cooled bolometers was in an early stage, and our experience with phonon-cooled bolometers was non-existent. There was no published literature on the use of SOI material for fabricating ultra-thin substrates, or on the integration of beam leads with
superconducting circuitry. To our knowledge, no other research group anywhere had fabricated devices on stand-alone substrates as thin as 3μm.

In addition to my work on ultra-thin silicon chips and beam leads, I spent a considerable amount of time developing two HEB fabrication processes. These processes utilize electron-beam lithography to define the nanometer-scale dimensions of the HEB microbridges. While such electron-beam lithography processes have been used by other research groups, our group had no experience with such techniques. In addition, the electron-beam lithography system was installed just as this work began, so I was the first user to implement our system.

I fully developed each of the processes for fabricating both diffusion-cooled and phonon-cooled HEBs, and I tailored these processes specifically to be compatible with ultra-thin silicon chips. My ultimate goal was to integrate the bolometer and ultra-thin chip processes together into a novel heterodyne mixer chip. The development of fabrication processes for ultra-thin silicon chips, as well as diffusion-cooled and phonon-cooled hot-electron bolometers, provides our research group with the ability to design and assemble wide-bandwidth heterodyne mixer receivers capable of operating at THz frequencies. These new technologies extend our capabilities beyond the current limits of our SIS mixer technology.

1.1 Heterodyne Mixing

Signals of interest to radio astronomers in the Terahertz band are generally weak (on the order of $10^{-15}$ W), and therefore must be amplified before spectroscopic analysis. However, low-noise amplifiers that operate beyond 150GHz currently do not exist.
Heterodyne mixing shifts the center frequency of these signals to a lower frequency where low-noise amplification is possible.

A mathematical understanding of heterodyne mixing is as follows. Of interest is the spectrum of a weak signal centered around a frequency, $\omega_{RF}$ (the radio frequency). When $\omega_{RF}$ mixes with a strong, local, sinusoidal signal of similar frequency, $\omega_{LO}$ (the local oscillator), a difference frequency is produced at the output of the mixer. This output signal is centered around $\omega_{IF}$ (the intermediate frequency). The spectrum around $\omega_{IF}$, if properly mixed, contains the frequency-shifted phase and relative amplitude information contained in the original RF signal. At the input of the mixer, the RF and LO signals appear as a sum, expressed in Equation 1.

\[
v_{in} = s_{RF}(t) \cos \omega_{RF}t + s_{LO}(t) \cos \omega_{LO}t
\]

Equation 1

where the $s_{xx}(t)$ functions are the complex envelopes of the RF and LO signals. This input voltage is applied across a nonlinear circuit element such as a diode, SIS junction, or bolometer. Ideally, the nonlinear circuit element has a strong higher-order harmonic in the Taylor Series expansion of its I-V characteristics. Applying the input signal across such a device will produce an output response due to the second harmonic, as described in Equation 2 for the case of the second order harmonic.

\[
v_o = A_0 v_{in}^2 = A_0 \left[ s_{RF}^2(t) \cos \omega_{RF}t + s_{LO}^2(t) \cos \omega_{LO}t \right]
\]

Equation 2

\[
= A_0 \left\{ s_{RF}^2(t) \cos^2 \omega_{RF}t + s_{LO}^2(t) \cos^2 \omega_{LO}t + 2s_{RF}(t)s_{LO}(t) \cos \omega_{RF}t \cos \omega_{LO}t \right\}
\]

Applying the law of cosines, the output is restated as follows.
\[ f_o = \frac{A_0}{2} \left\{ s_{RF}^2(t) + s_{LO}^2(t) + s_{RF}^2(t) \cos 2\omega_{RF}t + s_{LO}^2(t) \cos 2\omega_{LO}t \right\} \\
+ 2s_{RF}(t)s_{LO}(t) \left[ \cos(\omega_{RF} + \omega_{LO})t + \cos(\omega_{RF} - \omega_{LO})t \right] \]

Equation 3

If the output signal \( f_o \) then passes through a band-pass filter, the resulting output, \( f_{IF} \), is simply the down-converted portion of Equation 3, with \( \omega_{IF} = |\omega_{RF} - \omega_{LO}| \).

\[ f_{IF} = A_0 s_{RF}(t) s_{LO}(t) \cos(\omega_{RF} - \omega_{LO})t \]

Equation 4

Note that mixing is not limited to devices with a strong second harmonic. Other harmonics, especially the third harmonic, are also used in mixer designs. Third harmonic mixing commonly employs devices exhibiting anti-symmetric I-V characteristics, such as an anti-parallel set of Schottky diodes and SIS junctions.

1.2 Technology Limitations at THz Frequencies

The dimensions of elements in high frequency circuits become ever more critical as the receiver operating frequency is pushed higher into the THz domain. Lumped element approximations no longer hold as the wavelength of fields within a device decreases to around the scale of the circuit element. The design and placement of wire bonds, solder bumps and other circuit elements must take into account allowable tolerances in dimensions. For THz frequencies, these tolerances are extremely small, making receiver assembly difficult and highly susceptible to placement error.

In addition, the electrical characteristics of nonlinear mixing elements begin to degrade at high frequencies. For low-noise SIS junctions, the photon energies at THz frequencies exceed the gap energy of the superconductor, causing the superconductor to revert to its normal, lossy state. These and other issues are presented in this section in
order to point out the interest in researching novel device structures and chip packaging arrangements.

1.2.1 Submillimeter Circuit Limitations

Above the 700GHz limit, defined at around the superconducting gap frequency of niobium, the matching circuitry of niobium SIS receivers becomes lossy. Because of this, modifications in the traditional SIS architecture and development of new THz devices are subjects of modern THz research. Such advances are necessary to meet the bandwidth requirements called for in the designs of the next generation of radio astronomy observatories such as ALMA (Atacama Large Millimeter Array), the aircraft-based SOFIA (Stratospheric Observatory for Infrared Astronomy), and the European Space Agency’s space-based Herschel Observatory.

Several avenues of research are being explored in order to extend receiver capabilities beyond the gap frequency of niobium. To reduce loss in mixer tuning circuits, researchers are taking advantage of the low resistivity of aluminum to build the tuning elements in SIS mixer circuits for applications beyond 800GHz [14]. Superconducting compounds such as NbN and NbTiN have also been investigated for use in the mixer tuning circuitry due to the higher superconducting gap frequencies of these materials [15-18]. In addition, these materials have also been investigated for use in SIS junctions, with the goal of replacing the traditional niobium-based (niobium/aluminum-oxide/niobium) structure [19,20]. However, as with any superconducting material, NbN and NbTiN also have frequency limitations due to the respective superconducting gap frequencies, with limits of around 1.21THz and 1.23THz, respectively. Research of
novel devices for heterodyne mixing, such as hot-electron bolometers, aims to extend experimental capabilities of receivers into the THz frequency domain.

1.2.2 Limitations of Receiver Assembly

THz circuits are extremely small and usually fabricated on very thin and fragile substrate materials such as silicon or quartz. As the operating frequency of circuits increases, the size of the circuit housing decreases. In addition, the dimensional tolerances of the circuit housing decreases, making the placement of the circuit both more difficult and more critical. All of these problems make replicating state-of-the-art submillimeter-wave devices extremely difficult. To overcome these difficulties, the circuit mount has to be designed so that it is as simple as possible to assemble and non-critical to the function of the circuit. Also, the assembly procedures must be as clear and reliable as possible.

There are several critical design issues that need to be considered when developing both the circuit housing and the assembly procedures for THz receivers [21]. First, improper mounting techniques may mechanically damage chips and circuits. A small displacement of the chip in the receiver block may result in excessive loss, degradation of device sensitivity, or unwanted resonance. A good receiver block design should provide a robust mechanical interface for the fragile circuit. The housing must be simple to fabricate and non-critical to the circuit placement. It should also be easy to assemble, disassemble and reproduce. Second, while mounting submillimeter-wave circuits, any wiring lead or contact becomes a circuit element. An incorrectly sized or misplaced lead may de-tune the circuit or excite unwanted resonance. A small extra length of ground lead may result in decibels of loss. Improper electrical contacts increase
circuit loss, degrade device sensitivity and reduce reliability. Third, most seemingly mysterious device failures are actually caused by electro-static discharge (ESD). ESD most likely happens during the assembly process when the circuit is exposed to other objects that are on a different electrical potential. To avoid ESD, a suitable assembly environment and a proper mounting procedure need to be established and strictly followed.

This work attempts to address these issues by integrating hot-electron bolometer mixer circuits with new beam lead and ultra-thin chip technologies. Implementing these circuits on ultra-thin chips greatly simplifies the RF design process by limiting the amount of dielectric material within the microstrip channel of the waveguide. The beam leads provide electrical, thermal and mechanical contact between the circuit and the waveguide. Furthermore, a beam lead design reduces the complexity of the microstrip channel structure, and eases the process for making contact between the chip and the mixer block.

Integrating hot-electron bolometers onto these chips demonstrates two principles. First, the ultra-thin chip and beam lead technologies are viable techniques for mounting superconducting submillimeter-wave circuits within waveguide blocks. In this dissertation, we demonstrate techniques for integrating beam leads onto both quartz and ultra-thin silicon chips. Second, we can fabricate both diffusion-cooled and phonon-cooled hot-electron bolometers using the facilities and resources available at the University of Virginia.
1.3 References


Information Technologies, MMW and Sub-MMW Detectors, Solar Astrophysics, Non-EM Astronomy, Exo-Planet Detection, and Astrobiology, Waikoloa Village, Hawaii, August 2002


AlNx/NbTiN Junctions for SIS Mixer Applications,” *IEEE Transactions on Applied

“Performance of NbN Superconductive Tunnel Junctions as Mixers at 205GHz,” *IEEE

Chapter 2

State of the Art

Several technologies are discussed in this chapter in order to prepare the reader with a body of necessary background information. Presented first are several techniques for mounting submillimeter-wave circuits. Also discussed are the physics of both diffusion-cooled and phonon-cooled hot-electron bolometers. There is also a brief presentation of several of the nanometer fabrication techniques available at the University of Virginia. And finally, several HEB fabrication techniques used by other research groups are reviewed.

2.1 Submillimeter-wave Circuit Mounting Techniques

There are several ways to mount millimeter and submillimeter-wave circuits into receiver blocks. Conductive adhesive provides electrical contact and thermal heat sinking to some power device packages. After the adhesive is set, however, it is difficult to remove the circuit from the package without incurring damage. Also, applying the appropriate amount of adhesive at the intended places is not a simple task. Other microwave products commonly employ wire bonding and soldering. However, as the operating frequency of circuits increases, the electrical traces of the circuit shrink. Some of the circuit traces of millimeter and submillimeter-wave circuits are so small (less than 25µm) that it is very difficult to make a reliable bond to the circuit. Also, as the frequency increases, the required bond wire length becomes shorter and more critical. This makes attaching the leads to the circuit very difficult. In general, wire bonding and
soldering are used to assemble millimeter and submillimeter-wave circuits, but they are not without their share of difficulties.

Conductive adhesive, wire bonding, and soldering all attach leads permanently to the circuit. None are ideal for prototyping tasks where frequent changing of circuits is needed. Several other mounting techniques offer easy circuit replacement. SIS mixer chips often incorporate micro-spring contacts, which are formed by pressing a narrow (0.125mm in diameter) gold-plated beryllium-copper wire against the circuit contact pad [1,2]. However, micro-spring contacts are usually not as robust as those formed by wire bonding and soldering. Also, the initial fine adjustment of the micro-spring wire is very time-consuming. But since it is very easy to replace a circuit chip in a micro-spring contact package, this method is particularly useful in prototyping low-power dissipation devices.

Another popular mounting technique makes contact between the block and the circuit through conductive wire gaskets. This technique offers easy chip replacement capability and provides excellent mechanical, electric and thermal contact to the circuit. For example, our SIS mixer circuits are clamped between the top and bottom halves of a receiver block in a suspended-substrate stripline configuration. The RF and DC ground leads connect between the substrate and block through gold crush wires (the conductive gaskets). The wires sit atop shoulders that are milled along the lengths of the microstrip channel. The substrate sits atop these wires, with the wires contacting metal pads on the substrate. The wires compress between the block and the metal pads when the two halves of the block are brought into contact. Since the connections are made solely by compressing gold wires, the depth from the top surface of the lower half-block to the
shoulder of the substrate channel becomes very critical. Figure 1a shows a cross-sectional diagram of the conductive gasket technique. This technique has been applied successfully in packaging SIS mixers for many years at NRAO [3,4]. However, due to the difficulties in machining the shoulders along the microstrip channel with the precision required for high frequency applications, it may not be practical to use this technique in submillimeter-wave circuits.

![Figure 1](image_url)  

**Figure 1** Shown are cross-sectional diagrams through a microstrip channel, revealing the orientations of the chips within the channel. In (A), conductive gaskets connect the circuit on a chip to a waveguide block. The gaskets (gold) make contact between the chip (grey) and the block (copper) when the two block halves are clamped together. This technique is limited, however, by the dimensions of the shoulder; the dimensions demanded for submillimeter applications are often too small to be machined. In (B), beam leads provide electrical, thermal and mechanical contact between the chip and the waveguide. The beam leads (gold) are crimped between the block halves (copper), leaving the chip (grey) suspended within the middle of the waveguide. Chips featuring beam leads do not require small, complex structures along the sides of the microstrip channel.

A preferable method for packaging submillimeter-wave circuits is the beam lead technique. The beam lead technique was developed in the 1960's by Marty Lepselter at Bell Labs as a simple and reliable way for connecting integrated circuits to printed circuit boards [5]. In this approach, thick (1μm to 10μm) metal beam leads are formed directly on the circuit during the circuit fabrication process, becoming an integral part of the circuit. The metal lead patterns extend beyond the perimeter of the circuit. The beam lead circuits are usually packaged in a split-block housing. Using the beam lead as a handle, the circuit is picked up and placed into the substrate channel with the extended
beam beads positioned along the perimeter of the channel. As a result, the chip is suspended within the middle of the substrate channel. When the two halves of the block are brought together, the beam leads are clamped between the two block-halves. The beam leads provide good thermal and electrical connection to the device, and a rigid physical support for the chip. Figure 1b shows a cross-sectional diagram of the beam lead scheme. As shown, the beam leads are crushed between the block halves, securing the chip in place within the microstrip channel. The contact force is between the beam leads and the block halves, and not on the chip as other contacting methods require. As a result, beam leads allow for the use of thinner, more fragile substrates that might otherwise break when clamped between two block halves.

2.2 Hot-Electron Bolometers

For mixing applications beyond 1.2THz, HEBs are a good solution for heterodyne receiving. HEBs offer several advantages over SIS junctions and Schottky diodes. The RF (radio frequency) impedance is real and frequency independent. No LO (local oscillator) and RF harmonics are produced due to the slow thermal response of HEBs. Required LO power is very low (nano watts) and is frequency independent. The maximum operating frequency of HEBs is not limited by the device material.

Bolometer operation is based on the strong relationship that some materials exhibit between temperature and resistance. RF radiation, coupled to the absorber material of a bolometer, is converted to heat. The absorber has an electron specific heat capacity $C_e$, a thermal conductivity $G$ and is connected to a heat sink at a bath temperature, $T_{bath}$. The rise in temperature of the absorber material due to the incident RF and LO radiation results in a rise in electrical resistance. This corresponds to a change in
voltage across the absorber, if the bolometer is current biased ($I_{bias}$). Voltage sensitivity, $S$, is expressed in Equation 1 [6].

$$S = I_{bias} \frac{dR}{dT} G \frac{1}{\sqrt{1 + \omega^2 \tau_{th}^2}}$$  \hspace{1cm} \text{Equation 1}

The thermal response time, given by $\tau_{th} = C_v/G$, determines the speed of the bolometer.

Hot-electron bolometers based on superconducting materials have a high sensitivity due to the steep $dR/dT$ slope around the critical temperature of the superconductor. By biasing a bolometer around this steep transition, extremely sensitive, low-noise mixers with wide IF bandwidths may be achieved. In addition, the heat capacity of the electron gas is significantly smaller than the heat capacity of the lattice. At superconducting temperatures, the electrons are only weakly coupled to the lattice phonons. As a result, the RF power mainly heats the electrons, resulting in greater voltage sensitivity.

HEBs capable of operating at terahertz frequencies come in two varieties, which are differentiated by the dominant cooling mechanism of the bolometer. These are phonon-cooled HEBs (p-HEBs), where electron-phonon interactions dominate heat transfer, and diffusion-cooled HEBs (d-HEBs), where electron-electron interactions dominate. In this work, we are concerned with both types of bolometers.

### 2.2.2 Phonon-Cooled Hot-Electron Bolometer Theory

Gershenzon, et al first proposed the phonon-cooled hot-electron bolometer (p-HEB) in 1990 [7]. A p-HEB consists of a thin film of superconducting material between two metal pads. The spacing between the metal pads and the width of the pads is chosen such that the resistance presented by the thin film is matched to the RF antenna within which the bolometer is situated. The electrons in this film are excited by incident energy
from RF photons collected by the antenna. These excited electrons share their energy with other electrons in the film with a time period $\tau_{ee}$. As a result, a distribution of hot electrons is created within the film of the microbridge. These hot electrons in turn pass on their energy to phonons within a time period $\tau_{ph}$, the electron-phonon interaction time. If the film is thin enough, the phonons may escape into the substrate lattice within a short time period, $\tau_{ES}$.

In order for a distribution of hot electrons to build up within the film, $\tau_{ee}$ must be much less than $\tau_{ph}$. In addition, the phonons must escape to the substrate lattice ($\tau_{ES}$) before interacting again with another electron. In order for this to happen, the film must be very thin. The relationship between film thickness and $\tau_{ES}$ is shown by Equation 2.

$$
\tau_{ES} = \frac{4dC_e}{v\alpha C_{ph}}
$$

Equation 2

$C_e$ and $C_{ph}$ are the electron and phonon specific heats, $v$ is the velocity of sound in the lattice, $d$ is the lattice thickness, and $\alpha$ is coefficient of transmission of a phonon though the film-substrate interface.[8]

In a sufficiently thin film, $\tau_{ph}$ is much greater than $\tau_{ee}$ and $\tau_{ES}$, so the thermal response time of the bolometer is determined by $\tau_{ph}$. Bandwidth is related to the electron-phonon interaction time by the relationship $f = (2\pi\tau_{ph})^{-1}$. For a thin film of NbN, $\tau_{ph} \approx 15$ps at cryogenic (4K) temperatures, which gives a theoretical bandwidth of roughly 10GHz [9].

Films of NbN are typically deposited by DC magnetron sputtering in a reactive environment of argon and nitrogen [10]. For phonon-cooled hot-electron bolometer applications, NbN films are typically around 4nm thick and have a critical temperature
(T_c) of between 9K and 11K. The resistivity of the 4nm thick films in our p-HEBs is around 400 μΩcm.

### 2.2.2 Diffusion-Cooled Hot-Electron Bolometer Theory

The idea for the d-HEB was first proposed by Prober in 1993 [6]. The physical layout of a diffusion-cooled bolometer consists of a small absorber material, in our case a 10nm thick niobium microbridge, contacting cooling pads on opposite ends. These cooling pads are typically thick (greater than 50nm) gold structures, and are much wider than the absorber material. During operation of a d-HEB, photons collected by an antenna heat electrons within the microbridge. These electrons then rapidly diffuse out of the microbridge and into the cooling pads, which act as heat sinks. The pad-to-pad spacing must be very small so that electrons may diffuse out of the niobium absorber area and into the gold cooling pads in a time less than the electron-phonon interaction time. To ensure electrons diffuse out of the microbridge before interacting with the lattice, the length of the bridge should be on order of the electron diffusion length, $l_{e-e}$ [8,11].

\[
l_{e-e} = 2\sqrt{D \tau_{e-e}}
\]

Equation 3

From the literature, the diffusion constant ($D$) for a 10nm thick niobium film is around 1cm²/s [12]. The electron-electron interaction time is estimated to be ~100ps for a thin (dirty limit) film of niobium. This yields a bridge length of approximately $l_{e-e} \approx 200$nm. The actual bridge length may be longer than this, but should not exceed the electron-phonon interaction length, $l_{e-ph}$. 
The 3dB IF bandwidth roll-off may be estimated from the thermal response time using Equation 4. As stated previously, the thermal response time is a function of the specific heat capacity and the thermal conductivity of the microbridge ($\tau_{th} = C_v/G$).

$$f_{3dB} = (2\pi \tau_{th})^{-1}$$  \hspace{1cm} \text{Equation 4}

For a typical niobium HEB, the thermal response time is around 30ps, giving an IF bandwidth of around 5GHz. However, the self-heating effect within the bolometer reduces the thermal conductivity of the microbridge, and thereby reduces the IF bandwidth.

2.2.3 RF Operation

The normal-state (non-superconducting) resistance, $R_n$, of the microbridge is controlled by varying the length and width of the bridge. Ignoring the RF and LO complex envelopes, and simply evaluating the fundamental frequencies of these two inputs, the voltage presented to this resistance is

$$v(t) = v_{LO} \cos \omega_{LO} t + v_{RF} \cos \omega_{RF} t$$  \hspace{1cm} \text{Equation 5}

The instantaneous power dissipated in the microbridge is then

$$P(t) = \frac{v^2(t)}{R_n}$$  \hspace{1cm} \text{Equation 6}

$$P(t) = P_{LO} + P_{RF} + 2(P_{LO}P_{RF})^{1/2} \cos \omega_{RF} t$$

where

$$P_{LO} = \frac{v_{LO}^2}{2R_n} \quad P_{RF} = \frac{v_{RF}^2}{2R_n}$$  \hspace{1cm} \text{Equation 7}

Note that for a typical hot-electron thermal response time ($\tau_{th}$) the frequency response, $(2\pi \tau_{th})^{-1} = 5$GHz, the response time of the microbridge is too slow to support modes of
\omega_{RF}, \omega_{LO} and the up-converted frequency \omega_{LO+\omega_{RF}}, but will support the IF frequency, \omega_{IF}.

Using Equation 1, which describes the voltage responsivity (S) of the bolometer, along with Equations 7 and 8 (below), we can estimate the amplitude of the IF voltage response across the bolometer as a function of absorbed power [8].

\begin{equation}
    v_{IF} = 2S \sqrt{P_{LO} P_{RF}}
\end{equation}

\textbf{Equation 8}

\section*{2.3 Nanometer-Scale Fabrication at UVa}

Fabrication of HEBs requires two nano-scale lithographic processing steps, one to define the bridge width and a second to define the bridge length. The required tolerance of these lithographic patterns is on the order of +/- 10nm. However, the standard, deep ultra-violate (DUV) photolithographic systems available at the University of Virginia Semiconductor Device Laboratory (SDL) are not capable of achieving device feature resolutions lower than 0.5\mu m. For this reason, we have explored alternative lithographic fabrication processes outside of the SDL. We investigated three nano-scale fabrication processes for fabricating HEBs using tools available at the University’s Materials Science Department. Two of these processes employ a focused ion beam (FIB). The third, covered in detail in the next section of this chapter, relies on a recently acquired electron-beam lithography system.

The focused ion beam system is fundamentally similar to a scanning electron microscope (SEM) in that a focused, collimated beam of charged particles accelerates towards a sample surface due to a high voltage. The FIB uses gallium ions (Ga+) from a liquid-metal ion source instead of electrons. Upon striking the sample surface, the massive Ga+ impart energy onto the sample, causing material from the sample surface to
mill away. The secondary electrons ejected from the sample surface are collected and processed into an image, just as is done in an SEM. The FIB proves to be a useful fabrication tool since the position of beam may be precisely controlled to within several tens of nanometers. Using CAD software, the beam is rastered over the sample surface in a specific pattern, thereby milling that pattern into the sample. The spot size of the Ga\(^+\) beam is on the order of 8nm, resulting in resolutions suitable for HEB fabrication.

### 2.3.1 Direct FIB Fabrication

At UVa, we use the precise milling capability of the FIB to fabricate HEBs. In a multi-step process, metal masks are deposited atop the niobium and gold layers of the eventual HEB structures. Nanometer-scale patterns are then defined in these metal masks using the FIB. The metal masks then serve to define the HEB niobium and gold in subsequent reactive ion etch (RIE) processes [13]. Datesman has shown the FIB to be a useful tool for milling small sets of HEBs, and he has measured superconducting transition plots of resistance versus temperature for 15nm thick, 200nm long microbridge structures [14].

### 2.3.2 Microcontact Printing

Microcontact printing is a non-photolithographic method of pattern transfer, and is capable of nanometer-scale resolution [15-17]. An apt analogy is to that of a rubber stamp and inker pad. In this technique, an elastomeric stamp transfers an ink, often a thiol, on to a substrate. Where the stamp contacts the sample surface, the ink self-assembles and forms a monolayer of molecules. This monolayer serves as a mask against a subsequent wet chemical etch of the underlying material. Typically, patterning is done
on gold surfaces using a hydrophobic thiol ink. Upon contact of the stamp to the sample surface, the sulfur-terminated end of the thiol molecules bond weakly with the gold surface. Exposure to a cyanide-based etchant in a water solution removes the gold that is unprotected by the thiol, thereby transferring the pattern from the stamp to the gold [18,19].

Techniques for reproducing the nanometer-scale features of the master mold pattern on to an elastomeric stamp are well established [20]. Transferring nanometer-scale patterns from a stamp to a gold surface, however, depends on several complicating factors, including the type of ink used, how the ink is applied to the stamp, as well as the pressure and contact time used in the stamping process [21]. All of these issues become more critical when reproducing nanometer scale patterns.

Despite our success of reproducing nanometer-scale patterns, several complications with our microcontact printing process have hampered our implementation of the technology as an effective HEB fabrication tool [22]. Our pattern transfer process depends upon stamp pressure, which we find difficult to control accurately. Also, the defect tolerance of the gold wet etchant are adversely affected at times by an additive, 1-octanol, placed in the etchant that is actually intended to reduce defects. And finally, as of 2002 we were not able to stamp a large field of patterns effectively. However, by the time of printing this dissertation, researchers within the University’s Materials Science Department had developed a system capable of reproducing pattern fields as large as 1 cm in diameter.

All of these issues are solvable, given enough time to research the solutions. However, in June 2002 the Materials Science department at UVa installed an electron-
beam lithography (EBL) system onto their JOEL 840A SEM. This particular EBL system has a proven record for aiding in the successful fabrication of nanometer patterns. We have deferred the research into nanometer-scale microcontact printing in order to pursue the more promising EBL opportunity.

2.4 Electron-beam Lithography

We use electron-beam lithography (EBL) to pattern the nano-scale features of our diffusion- and phonon-cooled HEBs. EBL is the process of defining patterns in a radiation-sensitive material (the resist) using a precisely defined and accurately controlled beam of electrons. Exposure of the resist to the energetic electrons from the beam results in a change in the chemical structure of the resist. These changes in the resist may be described by either one of two cases. In one case, termed positive lithography, exposure reduces the molecular weight of molecules within the resist. These reduced molecular weight molecules then readily dissolve in a developer, leaving behind the unexposed regions of the resist. Such is the case with poly(methyl methacrylate) (PMMA). Chain scission occurs upon impact with high-energy electrons, thereby reducing the molecular weight of the long PMMA polymer chains. The resulting low molecular weight polymeric chains then dissolve in methyl isobutyl ketone (MIBK). The other possible case, termed negative lithography, results in an inverted exposure pattern. In this case, the electron-beam activates a sensitizer within a polymer, which promotes cross-linking within the polymer. Upon exposure to a developer, the denser cross-linked regions of the resist remain behind while the unexposed regions dissolve [23].
2.4.1 SEM Basics

The source of an electron beam is best explained by first describing the basic operation of a scanning electron microscope (SEM). The electrons in an SEM are produced in a vacuum system by passing a high current (called the filament current) through a filament, typically tungsten or LaB₆. The filament current produces an emission of electrons, which then accelerate away from the filament towards a sample surface using a high accelerating voltage. Accelerating voltages range from 20kV to 100kV for electron-beam lithography applications. As the electrons travel towards the sample, they pass through a series of condensers (magnetic lenses) and apertures located within a column, producing a narrow beam of electrons. The x-y scan coils within the column raster the beam across the sample surface. Electrons from the incident beam either scatter off the sample surface or cause secondary electrons within the material to be ejected from the sample. These scattered and secondary electrons are collected and processed into an image, which is projected onto a CRT.

2.4.2 Resolution Limits of EBL

The minimum width of an electron beam at the substrate surface may be as small as 1nm, depending on the capabilities of the SEM and the skill of the operator. The resolution limit of EBL, however, depends upon the resist material and the developer solvent. For PMMA, electron scattering within the resist allows for a resolution no greater than 3nm to 5nm [24,25]. These resolutions are achieved only in carefully controlled, highly specialized EBL systems. For a typical SEM, this limit is even higher, often around 10nm to 15nm.
The molecular weight of PMMA prior to exposure is a significant factor in the resolution limits of EBL. Typically, thin layers of PMMA ranging from 40nm to hundreds of nanometers thick are spin-coated across a sample. PMMA is commercially available in a wide range of molecular weight, from 50kg/mol to 950kg/mol and beyond. Choice of molecular weight depends largely on the specifics of the application. For PMMA to readily dissolve, the molecular weight must be reduced to less than 4kg/mol upon exposure. This requires an exposure dose of around 150μC/cm² or greater, independent of the initial molecular weight of the PMMA [26]. High contrast images resolve best when using a higher molecular weight PMMA (950kg/mol and beyond) because of the large difference between the chain lengths of exposed and unexposed regions within the resist. However, this rule-of-thumb is not always true as pattern geometry plays a significant role in resolution. For instance, developer-induced swelling can occur in high molecular weight PMMA, which may severely distort small patterns. For high pattern density applications, the minimum pattern resolution is often achieved using a mid-range molecular weight PMMA, thereby balancing the effects of polymer swelling with the desire for high contrast.

2.4.3 The Nanometer Pattern Generation System (NPGS)

For the UVa EBL fabrication processes, we use a writing system called the Nanometer Pattern Generation System (NPGS). NPGS interfaces with the x-y scan coils of a JOEL 840A Scanning Electron Microscope (SEM) to precisely control the electron beam location. Using NPGS, we can define complicated patterns in an electron beam-sensitive resist.
In addition to controlling the SEM scan coils, NPGS also controls stage motion and allows for beam blanking, making it possible to write complex patterns over areas larger than the field of view of the SEM. An alignment algorithm is also included with the system.

The alignment process begins by first imaging alignment marks on the wafer. The location of these marks is then compared to the layout of the marks as they appear in a CAD file. The CAD file also contains the patterns for the electron beam writing. The x-y displacement and the rotation misalignment of the alignment marks are then measured. Based on these offsets, a translation matrix and x-y offset are calculated and applied to the writing pattern. The pattern file is then recalculated using these corrections prior to writing with the beam.

2.5 A Review of EBL-Fabrication Methods for HEBs

Two groups have published the majority of research regarding the fabrication of diffusion-cooled hot-electron bolometers. The first group covered in this review is from the Jet Propulsion Laboratories in Pasadena, California. The second is from the Space Research Organization of the Netherlands, which is located in Groningen. Both of these groups use electron-beam lithography (EBL) in their fabrication processes. This chapter presents a literature review of these processes. Very little detailed information is available regarding p-HEB fabrication, and so a literature review of the subject is not included in this section [27].
2.5.1 The JPL Process

Bumble and LeDuc outline the JPL (Jet Propulsion Laboratories) EBL-based fabrication process for diffusion-cooled HEBs in their 1997 paper [28]. They fabricate bolometers on both quartz and silicon substrates using a self-aligning process that defines a large niobium extent under the gold cooling pads. The first fabrication step involves sputtering a metal bi-layer consisting of the HEB niobium, followed by a gold over-layer. The niobium thickness is 10nm, and they deposit their film using DC magnetron sputtering in an argon environment. They then thermally evaporate a gold layer in the same vacuum system. The gold serves as a capping layer, preventing the niobium from oxidizing during subsequent fabrication processes.

Next, optical lithography defines micron-scale alignment marks. The alignment marks, patterned via lift-off, consist of 90nm of gold atop 10nm of Ti. JPL’s electron-beam lithography system uses the alignment marks to precisely pattern the sub-micron features of the bolometer. The process requires two separate EBL writing steps to define the bridge length and width.

The first EBL step defines the bolometer bridge width. A bi-layer of PMMA resists, with molecular weights of 2.3Mg/mol (top) and 950kg/mol, is spun atop the wafer. Resist thickness are each 100nm. Baking is performed at 115C for 15 minutes after spinning each layer. After EBL exposure, a 25nm thick gold film is evaporated over the sample. The gold patterns that remain after lift-off serve as an etch mask for subsequent RIE process, which defines the niobium bridge width. Bridge widths range from 50nm to 200nm.
The second EBL process defines the gold cooling pad extents. The gold cooling pads align atop the gold masking strip; the separation between the gold cooling pads defines the bridge length, which ranges from 50nm to 300nm.

Next, a physical, argon-based etch removes the exposed 15nm of open-field gold atop the HEB niobium. The argon etch takes place within a reactive ion etcher, though this etch does not require reactive gases. The argon etch leaves 25nm of gold atop the bridge. Immediately afterwards, a CCl₂F₂-based RIE removes the open-field HEB niobium. After etching, the wafers are rinsed with water due to concern about chlorine contamination due to the CCl₂F₂-based RIE chemistry.

Next, the large antennae patterns are defined using conventional optical lithography. The antennae structures consist of 300nm thick gold atop a 3nm thick Ti adhesion layer and are realized using lift-off.

The final fabrication process involves removing the gold masking layer, and then insulating the HEB regions of the wafer with a SiOₓ. The SiOₓ patterns are defined first, using conventional lithography. Windows in the photoresist are patterned above the bolometers. The gold is then etched away from atop the HEB bridge using an argon and O₂ RIE process. The addition of O₂ into the argon etch results in a thin niobium oxide layer atop the bridge. Immediately after etching, a 40nm layer of SiOₓ is thermally evaporated atop the wafer. SiOₓ outside of the resist windows is removed during exposure to a lift-off solvent.

2.5.2 The SRON Processes

The SRON (Space Research Organization of the Netherlands) processes are similar to the JPL process. This is understandable, as a considerable amount of
cooperation has occurred between these two groups; Danny Floet, whose dissertation work centered on diffusion-cooled HEBs, spent several months in Pasadena working with HEB-related researchers at JPL.

2.5.2.1 SRON HEB Fabrication As Described by Floet

The first bolometers fabricated at SRON are described in the dissertation by Floet (2001) [29]. However, the fabrication description does not contain a significant amount of detail. The process begins by first sputtering 12nm of HEB niobium atop a fused quartz wafer. Note that Floet does not use a gold over-layer to prevent the niobium from oxidizing during the subsequent fabrication processes. After sputtering, a bi-layer of PMMA is spun over the sample. Each resist layer is baked for 10 minutes at 120C in an oven. EBL is then used to define the gold cooling pads in a lift-off process. Prior to evaporation of the gold cooling pads, an ion mill is performed to remove the native niobium oxide from atop the HEB niobium. Gold pad thickness is 75nm.

Following this first EBL step, the RF filter structures are patterned by optical lithography. The filters consist of 50nm of gold atop 70nm of niobium. A 6nm layer of aluminum is sputtered between the gold and the niobium to promote adhesion.

The niobium bridge is then defined using a combination of EBL and optical lithography to define patterns in PMMA. The sub-micron bolometer bridge is patterned using EBL. The wider areas of PMMA are exposed using deep-ultraviolet (DUV) lithography. The result is a narrow PMMA pattern. The PMMA bridge pattern serves as an etch mask during RIE of the underlying HEB niobium.
2.5.2.2 SRON HEB Fabrication As Described by Ganzevlez

After Floet’s work, other EBL-based HEB fabrication processes were developed at SRON. These are described in more detail in a dissertation by Ganzevlez (2002) [30]. Ganzevlez fabricated HEBs on high-resistivity silicon; his mixers were based on quasi-optical coupling.

The HEB fabrication processes described by Ganzevlez all begin with the definition of alignment marks. The marks are patterned using EBL in a bi-layer PMMA resist. The bi-layer consists of a 350kg/mol layer atop a 180kg/mol layer. Each layer is baked at 120C for 5 minutes after spinning. The bi-layer thickness is around 330nm. After pattern exposure and development, an O₂ plasma etch is used to de-scum the patterns prior to metal deposition. The gold marks consist of 75nm of gold atop a 6nm aluminum adhesion layer. Both layers are deposited by DC sputtering. Patterns are complete following lift-off.

At this point, Ganzevlez diverges the discussion into three different processes for fabricating HEBs. For the first two fabrication processes, square niobium patches, 5µm long on a side, are deposited on the wafer using the previously described EBL process. The thickness of the niobium patches is 12nm. Again, no gold over-layer is sputtered atop this HEB niobium to prevent oxidation as is done in the JPL process.

The first process described by Ganzevlez is a more detailed variation of the one described by Floet. Gold cooling pads are defined in the 350-180kg/mol PMMA bi-layer using EBL. Before gold deposition, an argon ion cleaning removes the niobium oxide. 15nm of gold are then sputtered atop the cleaned niobium. The wafer is then transferred
to an evaporation system where another 100nm layer of gold is deposited. The gold cooling pads are fully defined after lift-off.

The niobium bridge is define using a third EBL process, identical to that described by Floet, where a strip of PMMA is defined atop the bridge area, and serves as an etch mask in a subsequent RIE process. The bi-layer PMMA is slightly different from that used in previous steps, as both layers use 350kg/mol PMMA to avoid an undercut resist profile. Following pattern writing and developing, the niobium bridge is defined using a CF$_4$-based RIE. The PMMA masking layer is then removed using acetone.

The second HEB fabrication process described by Ganzevlez uses an aluminum layer as the etch mask during the niobium bridge definition process. For the step after the RF choke structures are defined, EBL is used to write a bridge pattern above the gold cooling pads in a bi-layer PMMA resist. A 30nm thick layer of aluminum is then sputtered over the sample, leaving a thin aluminum mask atop the niobium after lift-off. The niobium is then etched using a CF$_4$-based RIE. The large etch selectivity between aluminum and niobium ensures that the aluminum is not removed from atop the niobium bridge during the RIE process. The aluminum mask is then removed via wet etch using Shipley 351, which is a resist developer.

The third SRON process described by Ganzevlez borrows the gold over-layer idea from the JPL process. The HEB niobium patches are covered with a 15nm thick gold over-layer, before breaking vacuum. The gold layer serves to prevent oxidation of the HEB niobium during processing. Gold cooling pads and RF filter structures are then defined. Since an argon ion mill is not required before sputtering the cooling pad gold, the sputtered HEB niobium thickness is only 10nm rather than 12nm. The gold over-
layer ensures good electrical contact between the HEB niobium layer and the gold of the cooling pads and filter structures.

Just prior to beginning the niobium bridge definition process, the gold overlay is removed using an argon RIE process, without masking. A PMMA or aluminum mask is then used to define the niobium bridge, as previously discussed.

2.6 References


Chapter 3

Design of the 585GHz Receiver

The original basis of my design for the 585GHz HEB waveguide mixer block derives from a family of receivers designed for the Submillimeter Array (SMA) by researchers at the Harvard-Smithsonian Center for Astrophysics. The basic SMA mixer block design consists of two halves; a feedhorn half and a back short half. A quartz substrate containing an SIS junction and low-pass filter structures is suspended in a microstrip channel between the two halves, parallel to the block split plane. The feedhorn, located in the upper block half, is perpendicular to the split plane. A reduced-height waveguide couples the RF and LO radiation from the feedhorn to a bowtie antenna structure on the quartz chip. A backshort, located behind the bowtie antenna in the lower block half, terminates the reduced-height waveguide behind the antenna.

The first SMA receiver operates around a center frequency of 200GHz [1,2]. Additional SMA receivers, operating at 300GHz, 450GHz and 600GHz, are scaled versions of the 200GHz receiver [3-5]. Kawamura, et al., designed a similar receiver that operates around 800GHz. This receiver features a phonon-cooled hot-electron bolometer as the non-linear mixing element, and was used in the Heinrich Hertz Telescope atop Mt. Graham in Arizona [6]. Researchers at the Space Research Organization of the Netherlands and Delft University adopted this design as well, and now plan to use their design for bands 3 and 4 of the Heterodyne Instrument for the Far-Infrared (HIFI) on the Herschel Space Observatory [7]. Figure 1a shows a wire frame model of the 600GHz
SMA design. The 585GHz SOI HEB receiver that I developed for this dissertation is discussed in this chapter and compared to the 600GHz SMA receiver.

Figure 1b shows a wire frame model of my 585GHz SOI HEB receiver design (585). I made several major structural changes when adopting the 585 design from the SMA design. First, I replaced the 50μm quartz substrate in the SMA design with an ultra-thin silicon substrate. Second, the quartz substrate in the SMA design sits atop shoulders milled along the sides of the microstrip channel. Since gold beam leads suspend the ultra-thin silicon substrate within the channel, the shoulders are unwarranted. As a result, the microstrip channel of the 585 receiver has a truly rectangular cross-section. I also scaled the dimension of the SMA design by a ratio of 600/585 in order to accommodate the change in operating frequency. And finally, I rotated the orientation of the feedhorn so that the length of the feedhorn runs parallel to the mating faces of the block halves. In the SMA designs, the long axis of the feedhorn is perpendicular to the mating faces, which requires electroforming and a mandrel in order to define the feedhorn. With the feedhorn oriented parallel to the block mating faces, the feedhorn antennae becomes easier, and therefore less expensive, to machine.

![Figure 1](image)

**Figure 1** (a) The 600GHz SMA receiver, with the feedhorn oriented perpendicular to the split plane. (b) The 585GHz SOI HEB receiver with the feedhorn oriented parallel to the split plane.
3.1 Receiver Design

The discussion of the design process for the 585GHz HEB receiver is divided into four sections. These sections cover the design of the low-pass filter, the microstrip channel, the reduced-height waveguide, and the feedhorn.

3.1.1 Low-pass Filter

Segments of quarter-wavelength long microstrip circuit lines form the low-pass filter in the 585 receiver. The filter prevents the RF and LO signals from propagating though to the IF and ground ports, which are located at the ends of microstrip channel. The impedance of microstrip lines depends upon several factors, including substrate material, substrate thickness, and the width of the metal line [8].

Figure 2 Shown is a schematic diagram of a microstrip line. A metal strip of width $W$ is located atop a dielectric layer with thickness $d$ and dielectric constant $\varepsilon_r$. The dielectric separates the metal strip from a ground plane. The characteristic impedance of the microstrip line is determined by the $W/d$ ratio and $\varepsilon_r$.

Figure 2 shows a diagram of a microstrip structure consisting of a dielectric medium and a metal microstrip, with vacuum surrounding both. A microstrip circuit is modeled as a metal line within a homogenous medium by placing the metal strip within a homogenous medium a height ‘$d$’ above a ground plane. This hypothetical homogenous region replaces the air and dielectric regions of the microstrip, simplifying analysis. The dielectric constant of this homogeneous region is given by
\[
\epsilon' = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + \frac{12d}{W}}} \quad \text{Equation 1}
\]

where \(\epsilon_r\), \(d\) and \(W\) are the substrate dielectric constant, the dielectric thickness and the metal width, respectively [9].

Equation 2 gives the \(W/d\) ratio as a function of the substrate dielectric constant and characteristic impedance, \(Z_0\) [9,10]

\[
\frac{W}{d} = \frac{8e^A}{e^{2A} - 2} \quad \text{for } W/d < 2 \quad \text{Equation 2}
\]

\[
\frac{W}{d} = \frac{2}{\pi} \left\{ B - 1 - \ln(2B - 1) + \frac{\epsilon_r - 1}{2\epsilon_r} \left[ \ln(B - 1) + 0.39 - \frac{0.61}{\epsilon_r} \right] \right\} \quad \text{for } W/d > 2
\]

where

\[
A = \frac{Z_0}{60} \sqrt{\frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{\epsilon_r} \left( 0.23 + \frac{0.11}{\epsilon_r} \right)} \quad \text{and} \quad B = \frac{377\pi}{2Z_0\sqrt{\epsilon_r}}
\]

An alternating series high-impedance and low-impedance quarter-wave long microstrip lines forms a low-pass filter. If there are enough segments in the series, then the impedance seen at the beginning of the circuit is either a short circuit or an open circuit at the design frequency of the filter, and presents a reflection coefficient of +/-1.

\[\text{Figure 3} \quad \text{Shown is a schematic diagram of the first two quarter-wavelength section of a low-pass filter. The impedance } Z_{IN} \text{ approaches either zero (a short) or infinity (an open) as more segments are added.}\]
Equations 3 and 4 describe four possible combinations of alternating high and low-impedance segments. These equations refer to the nomenclature described in Figure 3. If there is an even number of quarter-wavelength segments in the filter, then the impedance at the beginning of the sequence is calculated using Equation 3.

$$Z_{\text{IN}} = \frac{Z_1^{2i}}{Z_0^{2i}} Z_{\text{end}}$$

**Equation 3**

where ‘i’ is an integer greater than zero that relates to number of impedance segments in the sequence; $Z_{\text{end}}$ is the terminating impedance at the end of the filter; $Z_0$ is the characteristic impedance of the first quarter-wavelength segment; and $Z_1$ is the characteristic impedance of the second. For equation 3, the number of elements in the filter is twice ‘i.’ If there are an odd number of segments in the filter, Equation 4 gives the impedance at the beginning of the sequence.

$$Z_{\text{IN}} = \frac{Z_0^{2i}}{Z_1^{2(i-1)}} \frac{1}{Z_{\text{end}}}$$

**Equation 4**

The number of elements in the filter for the Equation 4 case is $2(i-1)+1$.

A minimum $Z_{\text{IN}}$ is found using Equation 3 if $Z_1$ is less than $Z_0$. $Z_{\text{IN}}$ approaches zero as the number of elements in the sequence increases, resulting in a reflection coefficient, $\Gamma$, of -1. Equation 4 gives a maximum $Z_{\text{IN}}$ when, again, $Z_1$ is less than $Z_0$. $Z_{\text{IN}}$ approaches infinity as the number of segments increases giving a reflection coefficient of one. These relationships are plotted in Figure 4. Note that in the two cases for which $Z_1$ is greater than $Z_0$, Equations 3 and 4 still tend toward zero and infinity, though not as quickly as the cases just described.

In the 585GHz receiver design, the low-pass filter presents a short ($\Gamma = -1$) to the RF and LO signals at either end of the bowtie antenna. This short prevents the RF and LO
signals from propagating towards the IF and ground ports. Note that when a hot-electron bolometer serves as the nonlinear circuit element, higher-order harmonics are not generated during mixing. The slow thermal response of the superconducting microbridge does not permit the generation of harmonics greater than $f = 1/\tau_{th}$, where $\tau_{th}$ is the thermal relaxation time in the superconductor around $T_c$. As a result, only the RF and LO signals are considered when designing the low-pass filters.

![Figure 4](image.png)

**Figure 4** Shown are plots of Equations 3 and 4 as a function of the integer $i$, ($i>0$). Two cases diverge towards infinity, resulting in a reflection coefficient, $\Gamma = 1$, for the filter. The two other cases diverge towards zero, resulting in $\Gamma = -1$.

Equation 5 relates the physical lengths of the microstrip lines in the low-pass filter to the desired electrical length.

$$l = \frac{\theta c}{2nf\sqrt{\varepsilon_e}}$$  \hspace{1cm} \textbf{Equation 5}

where $f$ is the operating frequency, $c$ is the speed of light in a vacuum, $\theta$ is the electrical line length ($\lambda/4$ or $\pi/2$), and $\varepsilon_e$ is the effective dielectric constant of the microstrip system, as stated in Equation 1. The operating frequency, $f = 430\text{GHz}$, is the -3dB point of the filter. Note that $\varepsilon_e$ depends on the characteristic impedance, $Z_0$, of the microstrip.
line and the dielectric constant of the substrate. Table 1 shows some physical line lengths for a 90° long strip line atop a silicon substrate over a range of $Z_0$ values. As shown in Table 1, there is an 18% variation in physical line length for 90° microstrip lines of 10Ω and 90Ω, even though both are electrically a quarter-wavelength long.

<table>
<thead>
<tr>
<th>$Z_0$ (Ω)</th>
<th>$W/d$</th>
<th>$\epsilon_r$</th>
<th>physical line length (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>7.23</td>
<td>9.79</td>
<td>55.6</td>
</tr>
<tr>
<td>30</td>
<td>1.76</td>
<td>8.40</td>
<td>60.0</td>
</tr>
<tr>
<td>50</td>
<td>0.80</td>
<td>7.81</td>
<td>62.2</td>
</tr>
<tr>
<td>70</td>
<td>0.34</td>
<td>7.35</td>
<td>64.1</td>
</tr>
<tr>
<td>90</td>
<td>0.14</td>
<td>7.05</td>
<td>65.5</td>
</tr>
</tbody>
</table>

Table 1 Physical line length as a function of characteristic impedance, $Z_0$. Also shown are the W/d ratio and the effective dielectric constant of the microstrip line, which are used for calculating microstrip line width. The cut-off frequency for the low-pass filter is 430GHz.

The widths of the quarter-wavelength segments are calculated using the W/d ratio for a given $Z_0$ and substrate thickness. The 585GHz HEB receiver is designed to accommodate silicon chips of three different thickness: 3μm, 7μm, and 10μm. However, the same line lengths and widths are used in the filter structures for all three silicon designs. As a result, the $Z_{\text{high}}$ and $Z_{\text{low}}$ quarter-wave segments for each of the three silicon substrates are different. In addition, the cut-off frequency of the filter also changes due to changes in the electrical length of the segments, as dictated by Equation 5. The segment lengths are calculated for a 10μm thick substrate with a $Z_{\text{high}} = 50$Ω and a $Z_{\text{low}} = 11$Ω. Table 2 shows how $Z_{\text{low}}$ and $Z_{\text{high}}$ change as a function of substrate thickness. Also included in Table 2 is the $Z_{\text{IN}}$ of the low-pass filter as seen at the bowtie antenna.
<table>
<thead>
<tr>
<th>Silicon Substrate Thickness (µm)</th>
<th>( Z_{\text{high}} (\Omega) )</th>
<th>( Z_{\text{low}} (\Omega) )</th>
<th>( Z_{\text{IN}} (\Omega) ) (6 segment LPF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>50 (0.80)</td>
<td>11 (6.6)</td>
<td>1.0 x 10^-5</td>
</tr>
<tr>
<td>7</td>
<td>42 (1.14)</td>
<td>7.5 (9.4)</td>
<td>4.3 x 10^-6</td>
</tr>
<tr>
<td>3</td>
<td>22 (2.67)</td>
<td>3.6 (22)</td>
<td>5.3 x 10^-6</td>
</tr>
</tbody>
</table>

**Table 2**  

\( Z_{\text{high}} \) and \( Z_{\text{low}} \) characteristic impedances for low-pass filter segments on 10µm, 7µm and 3µm thick silicon substrates. In parenthesis next to the characteristic impedances are the \( W/d \) ratios. \( W_{\text{high}} \) and \( W_{\text{low}} \) are calculated for \( Z_{\text{high}} = 50 \Omega \) and \( Z_{\text{low}} = 11 \Omega \) on a 10µm thick silicon substrate. \( Z_{\text{high}} \) and \( Z_{\text{low}} \) for the 7µm and 3µm cases are calculated using the \( W/d \) ratio and Equation 2. \( Z_{\text{IN}} \) is based on a six segment low-pass filter, and is calculated using Equation 3.

The low-pass filters for the 585GHz HEB receiver consist of six segments, three low-impedance sections and three high-impedance sections. Initial evaluations of various low-pass filters were made using Puff, a microwave simulation program. The simulations show a wide stopband in the \( s_{21} \) plot, ranging from around 300GHz to 900GHz, with a -50dB attenuation at 585GHz.

**3.1.2 Bowtie Antenna Design**

The geometry of the bowtie antenna is adjusted to match the impedance of the bolometer, which sits in the middle of the antenna. Two dimensions of the bowtie antenna affect the real and imaginary components of the impedance that is seen by the HEB. These are the bowtie taper angle and the flag length, which are shown in Figure 5 atop a photograph of an actual antenna.
Figure 5  The flag length and bowtie taper angle are shown superimposed on this photograph of a bowtie antenna. The bolometer (too small to see) is situated between the two bowtie halves, in the middle of the antenna. The two parameters are adjusted such that the real part of the impedance as seen by the HEB is maximized while the imaginary component is minimized. The taper angle of the bowtie in the Figure is 45° while the flag length is 26μm.

The taper angle describes the angle that the bowtie antenna follows between the bolometer and termination at the flag. The flag is a rectangular section of microstrip line that extends off the back end of the bowtie, opposite the location of the bolometer. The bowtie may be modeled as two short sections of transmission line connected in series to the bolometer. The first section, adjacent to the bolometer, models the flair angle of the bowtie taper. Changing the taper angle simply changes the characteristic impedance of the model transmission line. The second section of transmission line models the flag length. The electrical length of the transmission line varies as the physical length of the flag changes.

Adjusting the taper angle and flag length result in variations in both the real and imaginary components of the impedance. Figures 6 and 7 demonstrate how the real and imaginary components change as a function of these two parameters. The taper angle and the flag length are adjusted such that the imaginary component of the impedance is
near zero while the real part is maximized. Table 3 summarizes the taper angle and flag length of the 3µm, 7µm and 10µm silicon designs, along with those for the SMA design.

![Real and Imaginary Impedance vs Flag Length](image1)

**Figure 6** When the flag length of the bowtie antenna is adjusted, the real and imaginary components of the impedance change. Ideally, the imaginary part of the impedance is near zero. The taper angle of the bowties simulated for this Figure are all 61°.

![Real and Imaginary Impedance vs Taper Angle](image2)

**Figure 7** The taper angle of the bowtie also has an effect on the impedance seen by the bolometer. The flag lengths of the bowties simulated for this Figure are all 35µm long.
<table>
<thead>
<tr>
<th>Design</th>
<th>Taper</th>
<th>Flag Length ($\mu$m)</th>
<th>$Re{Z}$ ($\Omega$)</th>
<th>$Im{Z}$ ($\Omega$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMA</td>
<td>68°</td>
<td>17</td>
<td>45.6</td>
<td>-5.2</td>
</tr>
<tr>
<td>31a(3$\mu$m)</td>
<td>45°</td>
<td>26</td>
<td>33.4</td>
<td>-1.5</td>
</tr>
<tr>
<td>32a(7$\mu$m)</td>
<td>45°</td>
<td>16</td>
<td>32.1</td>
<td>-0.7</td>
</tr>
<tr>
<td>33a(10$\mu$m)</td>
<td>45°</td>
<td>13</td>
<td>29.1</td>
<td>0.8</td>
</tr>
</tbody>
</table>

Table 3 Flag length and taper angle are presented for the three 585GHz designs as well as for the SMA design. The resulting real and imaginary components of the impedance that are seen by the bolometer are shown in the rightmost columns.

3.1.3 SOI LPF Microstrip Channel

The low-pass filter and bowtie antenna are fabricated atop an ultra-thin silicon substrate. This substrate is placed within a microstrip channel to prevent coupling from the microstrip to external sources. The dominant mode in a shielded microstrip is a quasi-TEM mode, which has no cut-off frequency [9, pp. 140]. The fields of the dominant mode are confined around the metal microstrip. Higher-order modes tend not to concentrate around the microstrip; the presence of higher-order modes complicates circuit analyses. All higher-order modes have cut-off frequencies, which are a function of the waveguide dimensions. By selecting the appropriate dimensions for the microstrip channel, propagation of these higher-order modes is eliminated [11]. In order to simplify circuit design, the dimensions of the microstrip channel are chosen such that the higher-order modes cannot propagate within the microstrip channel. As a result, only the dominant mode is considered during design.
Figure 8 Across-section along the width of a microstrip channel. The silicon substrate is placed within the channel such that the top of the silicon is in the electrical middle of the channel. The dimensions of W and $H_{\text{Tot}}$ are around a quarter-wavelength.

Figure 8 shows a cross-section of the microstrip channel, including the ultra-thin silicon substrate. In order to find the appropriate dimensions for the microstrip channel, the dimensions of a 585GHz waveguide channel initially designed by Hesler were used as a starting point [8]. In Hesler’s design, the height of the waveguide channel is a little less than a quarter of a wavelength, or $128\mu m$ at 585GHz. The microstrip channel is designed for a 40$\mu m$ thick quartz chip, which fills the lower half of the waveguide. The metal microstrip line is placed near the electrical center of the channel. As a result, the lower channel is shallower than the upper channel ($40\mu m$ and $64\mu m$, respectively), but the result is still an electrical quarter-wavelength height for the channel.

The dimensions of the microstrip channel are optimized by varying the waveguide height and width until the high order modes are eliminated from the operational band. The silicon chip is placed such that the metal microstrip is near the electrical center of the
channel. Referring to Figure 8, Equation 6 expresses the relationship between $H_{hi}$ and $H_{lo}$ of the waveguide.

$$H_{hi} = \sqrt{e_r} H_{St} + H_{lo}$$ \hspace{1cm} \textbf{Equation 6}

Each variation is simulated using HFSS (High Frequency Structure Simulator, Ansoft Co.) until a geometry that maximizes the frequency onset of both the second and third order modes is obtained. Table 4 shows the results of these simulations. The values in the last row of Table 4 are used in the 585GHz HEB receiver design.

<table>
<thead>
<tr>
<th>File Name</th>
<th>$W$ (μm)</th>
<th>$H_{lo}$ (μm)</th>
<th>$H_{hi}$ (μm)</th>
<th>$H_{Tot}$ (μm)</th>
<th>Mode 2 (GHz)</th>
<th>Mode 3 (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>585_08</td>
<td>110</td>
<td>26</td>
<td>50</td>
<td>96</td>
<td>340</td>
<td>860</td>
</tr>
<tr>
<td>585_09</td>
<td>100</td>
<td>31</td>
<td>65</td>
<td>106</td>
<td>510</td>
<td>810</td>
</tr>
<tr>
<td>585_11</td>
<td>90</td>
<td>31</td>
<td>65</td>
<td>106</td>
<td>600</td>
<td>800</td>
</tr>
<tr>
<td>585_13</td>
<td>80</td>
<td>31</td>
<td>65</td>
<td>106</td>
<td>680</td>
<td>800</td>
</tr>
<tr>
<td>585_14</td>
<td>86</td>
<td>31</td>
<td>65</td>
<td>106</td>
<td>640</td>
<td>800</td>
</tr>
<tr>
<td>585_15</td>
<td>86</td>
<td>33</td>
<td>67</td>
<td>110</td>
<td>620</td>
<td>780</td>
</tr>
<tr>
<td>585_16</td>
<td>86</td>
<td>29</td>
<td>63</td>
<td>102</td>
<td>590</td>
<td>820</td>
</tr>
<tr>
<td>585_17</td>
<td>84</td>
<td>31</td>
<td>65</td>
<td>106</td>
<td>620</td>
<td>800</td>
</tr>
<tr>
<td>585_18</td>
<td>88</td>
<td>31</td>
<td>65</td>
<td>106</td>
<td>600</td>
<td>800</td>
</tr>
<tr>
<td>585_19</td>
<td>86</td>
<td>32</td>
<td>66</td>
<td>108</td>
<td>640</td>
<td>780</td>
</tr>
<tr>
<td>585_20</td>
<td>80</td>
<td>29</td>
<td>63</td>
<td>102</td>
<td>670</td>
<td>820</td>
</tr>
</tbody>
</table>

\textbf{Table 4} Dimensions for various microstrip waveguide channels simulated using HFSS. The dimensions were optimized such that the mode 2 and 3 cut-off frequencies (rightmost columns) were as high as possible. A 10μm thick silicon substrate is used in all simulations. The substrate is oriented such that the gold microstrip is at the electrical middle of the waveguide. The values in the last row are used in the 585GHz HEB receiver design.

\textbf{3.1.4 Reduced-Height Waveguide and Backshort}

In the 585GHz HEB receiver, a reduced-height waveguide couples the RF and LO signals from the feedhorn of the receiver to the bowtie antenna. The dimensions of the waveguide are scaled from the 600GHz SMA design; the dimensions are 383μm wide by 93μm high. In the SMA design, the waveguide is oriented with respect to the microstrip channel perpendicular to the plane of the silicon chip. The original design for the 585
receiver also orients the feedhorn with the microstrip channel in this manner. However, such an arrangement presents difficulties for machining the block. To ease the machining process, a second design is used, which has the feedhorn oriented parallel to the plane of the microstrip channel, as shown in Figure 1. This design change is discussed later on in this chapter.

On the other end of the bowtie antenna is a backshort with the same dimensions as the reduced-height waveguide. The distance from the end of the backshort to the metal of the microstrip line is 128μm, or one quarter-wavelength at 585GHz in free space. The quarter-wave long backshort presents an open circuit impedance at the bowtie. The infinite impedance results in \( \Gamma = 1 \) at the bowtie. The \( \Gamma = 1 \) reflection coefficient maximizes the electric field potential across the bowtie, resulting in a maximum power transfer from the source to the bolometer.

If the backshort is improperly designed or poorly machined, variation in the backshort length may affect the power coupling to the bolometer. To investigate the robustness of the backshort in the 585 design, HFSS simulations were run for waveguide structures with various backshort lengths. In the HFSS simulations, a small coaxial probe is attached to the middle of the bowtie and the impedance is calculated by measuring the \( s_{11} \) reflection at that port. Table 5 shows the results from the simulations. Variations in backshort length by as much as +/- 15μm do not adversely affect the impedance seen by the bolometer.
<table>
<thead>
<tr>
<th>Length (µm)</th>
<th>Re{(s_{11})}</th>
<th>Im{(s_{11})}</th>
<th>Re{(Z)} (Ω)</th>
<th>Im{(Z)} (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>113</td>
<td>-0.400</td>
<td>0.044</td>
<td>33.2</td>
<td>3.5</td>
</tr>
<tr>
<td>118</td>
<td>-0.406</td>
<td>0.017</td>
<td>32.7</td>
<td>1.4</td>
</tr>
<tr>
<td>123</td>
<td>-0.391</td>
<td>0.004</td>
<td>33.9</td>
<td>0.3</td>
</tr>
<tr>
<td>128</td>
<td>-0.397</td>
<td>-0.019</td>
<td>33.5</td>
<td>-1.5</td>
</tr>
<tr>
<td>133</td>
<td>-0.387</td>
<td>-0.044</td>
<td>34.2</td>
<td>-3.6</td>
</tr>
<tr>
<td>138</td>
<td>-0.392</td>
<td>-0.054</td>
<td>33.7</td>
<td>-4.3</td>
</tr>
<tr>
<td>143</td>
<td>-0.390</td>
<td>-0.072</td>
<td>33.7</td>
<td>-5.7</td>
</tr>
</tbody>
</table>

*Table 5* Measurements of \(s_{11}\) as a function of backshort length and the calculated real and imaginary parts of the impedance seen by the bolometer. The backshort is specified as 128µm in the design of the 585GHz HEB receiver, but variations by as much as 15µm in either direction do not significantly affect the impedance.

### 3.1.5 Diagonal Feedhorn

A diagonal feedhorn couples the RF and LO radiation from the source to the reduced-height waveguide. The feedhorn is a scaled version of a feedhorn from a 600GHz SIS receiver, designed for the Atacama Large Millimeter Array [12]. HFSS simulations of the feedhorn, when connected to a reduced-height waveguide, show that the impedance at the open end of the horn is 377Ω.

### 3.2 HFSS Simulations

Microwave simulations of receiver designs made using HFSS predict several parameters of the waveguide structures. These include the port impedances, higher-order mode propagation, impedance at the bowtie antenna, and field distributions within the mixer structure. Iterative adjustments to the dimensions of the mixer components, based on the outcomes of previous simulations, are analyzed until an optimum solution is achieved [13].

HFSS is a 3D EM field simulation tool that allows the user to build and simulate a microwave structure within a 3D environment. A host of 3D CAD tools, along with a large materials database, facilitates accurate simulations of complex structures. EM field
distributions within the structures are solved using an adaptive finite-element mesh routine, which is refined iteratively until a user-defined convergence is met. The field solutions generated by this algorithm accurately predict high-frequency behavior. We use these solutions in this work to predict mixer behavior as a function of geometry and materials.

With HFSS, adjustments to the physical structure of the mixer are made using the 3D modeler. For the receiver designs discussed in this dissertation, the mixer geometries are divided along symmetry planes to reduce processing time. With properly chosen symmetry divisions, simulation results are achieved within a reasonable timeframe, allowing for the modeling of many fine structural modifications.

3.2.1 585 Upright Receiver Design

The first simulations were made of the SMA-like, upright feedhorn design. Prior to considering the ease of fabricating a mandrel for electroforming of the upright feedhorn, this design was optimized for three silicon chip microstrip circuits: the 3µm, 7µm and 10µm thick silicon chips. Each design is optimized such that a real impedance is presented to the bolometer at the bowtie antenna. Reactance is tuned out by adjusting the flag length of bowtie antennas, L1. Table 6 shows the parameters for the three optimized designs.
In order to calculate the real and imaginary components of the impedance, \( Z \), at the bowtie antenna, a small section of coaxial waveguide is constructed within HFSS to contact the bowtie. The s-parameter \( s_{11} \) is measured at this port, and from Equation 7, \( \text{Re}\{Z\} \) and \( \text{Im}\{Z\} \) are calculated.

\[
Z = Z_{\text{coax}} \frac{1 + s_{11}}{1 - s_{11}}
\]

Both \( Z \) and \( s_{11} \) are complex. The parameter \( Z_{\text{coax}} \) is the characteristic impedance of the coaxial probe. The flag length, \( L1 \), is adjusted iteratively until a minimum \( \text{Im}\{Z\} \) is achieved. The calculated \( \text{Re}\{Z\} \) is the impedance seen by the bolometer; for maximum power transfer from the antenna to the bolometer, the length and width of the microbridge is chosen such that the resistance of the microbridge equals \( \text{Re}\{Z\} \).

In order to reduce calculation time, the mixer structure for the upright feedhorn design is divided into quarters along E- and H-planes of symmetry. Figure 9 shows a wire frame model of the 3D structure, with an inset showing the coaxial probe contacting the tip of the bowtie antenna.
In addition to using HFSS to calculate the port impedances at 585GHz, the frequency response of the design is modeled over the range of 10GHz to 1THz. From this sweep, the s-parameters of the mixer are acquired as a function of frequency. A few of these are of considerable importance, including the magnitudes of $s_{31}$, $s_{22}$, and $s_{21}$ of the dominant mode. In addition, $s_{11}$ is plotted on the Smith chart to observe how the impedance at the bowtie antenna changes as a function of frequency. Because the upright
feedhorn design is not used in the 585 receiver, analysis and plots of these parameters are deferred to the discussion of the 90° feedhorn receiver design.

### 3.2.2 90° 585 Design

To ease machining of the waveguide block, the long axis of the feedhorn in the 90° 585 design is placed along the split plane of the block. Note that this orientation does eliminate the symmetry along the E-plane of the mixer. As a result, HFSS simulations are conducted on a model divided in half along the H-plane of symmetry, which bisects the reduced-height-waveguide. Figure 10 shows a wire frame model of the 90° 585 design that was constructed for simulation in HFSS. As with the upright design, a coaxial probe is included within the model to contact the bowtie antenna at the bolometer location. The inset in the upper left of Figure 10 shows the coaxial connection contacting the bowtie antenna.
HFSS wire frame model of the 90° 585 design. The model is only one-half of the actual design, and is divided along E plane of symmetry (bisecting the reduced-height waveguide) to decrease computation time. The inset in the upper left shows a close-up of the coaxial probe, which connects to the end of the bowtie antenna for $s_{11}$ measurements.

Figure 10  

HFSS simulations show very little difference in frequency response and port impedances between the upright and 90° designs. Figure 11 shows the $s_{31}$ response for both the upright feedhorn design and the 90° feedhorn design for a 3μm thick silicon substrate. The bandwidth of each design is roughly the same, and the curve forms are nearly identical.

Changing the orientation of the feedhorn from the upright structure to the 90° structure does not require re-design of the microstrip channel. As for the dimensions of the bowtie structures, only a slight modification is made to the 10μm silicon design to minimize $\text{Im}\{Z\}$ at the bowtie. The 3μm and 7μm designs are identical to those used in
the upright design. Table 7 shows the bowtie dimensions and the associated calculated impedances at the bowtie antenna.

![Figure 11](image)

**Figure 11** The magnitude of $s_{31}$ is plotted versus frequency for both the upright feedhorn design and the 90° offset design. The above plot shows that receiver performance is not impaired when the feedhorn is oriented along the split plane of the block.

Frequency measurements of the 90° receiver design show the s-parameter responses of the waveguide. Of interest are the magnitudes of $s_{31}$, $s_{22}$, and $s_{21}$ as functions of frequency, and $s_{11}$ plotted on the Smith chart. Referring to Figure 10, port 1 is the coaxial connection to the bowtie, port 2 is the input to the reduced-height waveguide, and port 3 is the far left end of the microstrip channel.

<table>
<thead>
<tr>
<th>Pattern Name</th>
<th>Silicon Thickness</th>
<th>Bowtie Taper</th>
<th>$L_1$ ($\mu$m)</th>
<th>Re{$Z$} ($\Omega$)</th>
<th>Im{$Z$} ($\Omega$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>33a</td>
<td>10(\mu)m</td>
<td>45°</td>
<td>13</td>
<td>29.1</td>
<td>0.3</td>
</tr>
<tr>
<td>32a</td>
<td>7(\mu)m</td>
<td>45°</td>
<td>16</td>
<td>32.1</td>
<td>-0.7</td>
</tr>
<tr>
<td>31a</td>
<td>3(\mu)m</td>
<td>45°</td>
<td>26</td>
<td>33.5</td>
<td>-1.5</td>
</tr>
</tbody>
</table>

*Table 7* Design parameters and calculated impedance values for the 3\(\mu\)m, 7\(\mu\)m and 10\(\mu\)m thick silicon chips at 585GHz in the 90° receiver design.
The $s_{31}$ response measures transmission of the dominate mode from the bowtie antenna to the IF and RF ground ports. If the low-pass filter and microstrip channel are properly designed, the low-pass filter blocks propagation below the operating frequency of the filter. Such a response is seen in Figure 12, which plots the $s_{31}$ magnitude versus frequency for the 3μm, 7μm and 10μm designs.

![Figure 12](image)

**Figure 12** Plotting the magnitude of $s_{31}$ verses frequency shows the coupling between the IF port (port 3) and the bowtie antenna (port 1). The stepped-impedance low-pass filter in the microstrip channel prevents the RF and LO signals from propagating through the microstrip channel to the IF and RF ground ports. Above, $|s_{31}|$ is plotted for the 3μm, 7μm and 10μm designs. Note the change in cut-off frequency as a function of substrate thickness; the electrical lengths of the filter segments change slightly as the substrate thickness changes, which in turn affects the cut-off frequency.

The $s_{21}$ response measures the coupling between the reduced-height waveguide and the bowtie antenna. The RF and LO signals should couple from the waveguide to the bowtie antenna without experiencing significant transmission loss throughout the band of interest, roughly 540GHz to 620GHz. Figure 13 shows the magnitude of $s_{21}$ as a function of frequency for the three silicon chip designs. As shown, very little transmission loss occurs in the band around the 585GHz operating frequency.
Figure 13 Plotting the magnitude of $s_{21}$ verses frequency shows the coupling between the reduced-height waveguide (port 2) and the bowtie antenna (port 1). Above, $|s_{21}|$ is plotted for the 3μm, 7μm and 10μm designs.

Figure 14 The plot of the magnitude of $s_{22}$ verses frequency shows the transmission window of the reduced-height waveguide (port 2). The waveguide band must be wide enough to accommodate the RF and LO signals. Above, $|s_{22}|$ is plotted for the 3μm, 7μm and 10μm designs.
The magnitude of $s_{22}$ as a function of frequency shows the propagation characteristics of the reduced-height waveguide, and is largely independent of the rest of the mixer circuit. The reduced-height waveguide is designated as port 2 and the $s_{22}$ response is plotted in Figure 14. Above a cut-off frequency of roughly 400GHz, the reduced-height waveguide has a purely resistive characteristic impedance, and so permits propagation of RF signals. Above cut-off, the reflected signal is minimized, so $s_{22}$ has a very small magnitude. Below the cut-off frequency, the reduced-height waveguide presents a purely reactive characteristic impedance. Therefore, all incident signals reflect back towards port 2, resulting in a unity $s_{22}$ magnitude. The simulation plots of the magnitude of $s_{22}$ as a function of frequency show these characteristics. All three silicon chip designs produce near-identical frequency responses.

As previously discussed in this chapter, the impedance of the mixer as seen at the bowtie antenna may be calculated from $s_{11}$ measurements. Table 7 gives the value of this impedance, $Z$, at the operating frequency. The microstrip circuitry is optimized such that the imaginary part of $Z$ is eliminated. Just as importantly though is the frequency response of $s_{11}$ over a broad frequency range. Ideally, $s_{11}$ does not vary significantly over the band of interest. Plotting $s_{11}$ on the Smith chart is useful for determining the behavior of $Z$ as a function of frequency. Figure 15 shows $s_{11}$ plotted on a Smith chart over two frequency bands for each of the three silicon designs. Between 400GHz and 820GHz, all three designs show large variations in $s_{11}$, shown in Figure 15 as the thin lines. However, between 540GHz and 620GHz, within the operational bandwidth of the bolometer, there is very little variation in $s_{11}$. This band is shown as the bold lines in Figure 15. The lack
of variation in $s_{11}$ indicates that the bolometer, if fabricated correctly, remains well matched to the mixer within the operational band of the bolometer.

![Smith Chart](image)

**Figure 15** The parameter $s_{31}$ is plotted on the Smith Chart for the 3\(\mu\)m, 7\(\mu\)m, and 10\(\mu\)m design cases. The thin plot lines sweep from 400GHz to 820GHz. The bold plot lines sweep from 540GHz to 620GHz, and represent the approximate operational band of the mixers. As is shown in the 7\(\mu\)m and 10\(\mu\)m cases, there is little variation in $s_{31}$ through this narrow band, implying that the impedance seen at the bowtie antennae is rather stable through the operational band of the receiver. The 3\(\mu\)m case shows slightly more variation within the band.

### 3.2.3 Spatial Variations in Chip Location and Backshort Length

In order to predict how the mixer would behave if chip placement or waveguide dimensions were to deviate from the design, a number of simulations were run with offsets built into the model. In Figure 16, three Smith charts show the effects of some potential design deviations. None of the simulations demonstrates failure by the mixer for any of the offsets modeled. In fact, the modeled deviations produced little to no variation in the $s_{11}$ response of the mixer.
Figure 16 In order to predict the behavior of the receiver if chip placement or backshort distance were to deviate from design, simulations were run in HFSS with several of these offsets modeled. In the upper left is a Smith chart showing how the $s_{11}$ frequency response changes when the chip placement deviates along the $z$-axis by $\pm 4.5\mu m$ (the chip is too high or too low within the microstrip channel). In the upper left, offsets in chip placement along the $x$-axis by $\pm 4.5\mu m$ are modeled (the direction parallel to the length of the feedhorn antenna). The Smith chart in the bottom center demonstrates $s_{11}$ variation for backshort lengths that are offset by $\pm 10\mu m$. None of the simulations indicates significant deviation in $s_{11}$ when these parameters are varied. Note that it was not possible to measure chip offset along the length of the microstrip channel ($y$-axis) due to a breakdown in model symmetry and difficulty in placement of the coaxial probe within the HFSS model.

3.2.4 Substituting Quartz for Silicon

RF simulations of the three circuit designs were run with quartz substituted for the silicon substrates. This was done in order to determine if any of the circuits could be adapted for use on a quartz substrate. If so, then it would be possible to test circuits on quartz substrates with the 585GHz receiver design, and then compare performance between mixers on quartz substrates and mixers on ultra-thin silicon substrates. Simulations were run using a variety of quartz thickness until the optimal thickness was
found. RF simulations were run in HFSS with substrate thickness ranging from 25\(\mu\)m to 39\(\mu\)m, the full height of the lower half of the microstrip channel.

All three circuit designs are adaptable to quartz substrates. The best performance in all three cases occurred when using 30\(\mu\)m thick quartz substrates. However, the frequency band over which the circuits worked best varies with respect to the silicon designs, and with each other. Figure 17 shows a Smith chart with the \(s_{11}\) parameter plotted as a function of frequency for the three optimal designs. For comparison, the \(s_{11}\) response of the 3\(\mu\)m silicon design is also included. All three designs match well on quartz substrates over very wide bands, which are highlighted in bold in the Figure. The impedances and optimal center frequencies are summarized in Table 8.

Figure 17 The three circuit designs for ultra-thin silicon chips were tested on 30\(\mu\)m thick quartz substrates in HFSS. The designs adapt well to the substrate change, though there is a shift in the operational band for each of the three designs.
### Table 8

<table>
<thead>
<tr>
<th>Pattern Name</th>
<th>Quartz Thickness</th>
<th>Re{Z} (Ω)</th>
<th>Im{Z} (Ω)</th>
<th>Optimal Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>31aQtz</td>
<td>30μm</td>
<td>40.7</td>
<td>0.2</td>
<td>680GHz</td>
</tr>
<tr>
<td>32aQtz</td>
<td>30μm</td>
<td>33.0</td>
<td>-0.9</td>
<td>740GHz</td>
</tr>
<tr>
<td>33aQtz</td>
<td>30μm</td>
<td>23.0</td>
<td>-0.4</td>
<td>700GHz</td>
</tr>
</tbody>
</table>

Shown are the summaries of optimal performance from the three circuit designs that were tested on 30μm thick quartz substrates.

### 3.3 Block Design

After I designed and simulated the 585GHz receiver in HFSS, I drafted the entire receiver block assembly in AutoCAD. The mixer block consists of two pieces, a top half and a bottom half, which are divided through the middle of the diagonal feedhorn. Figure 18 shows the AutoCAD schematics of the assembled block halves. A 50Ω SMA coaxial flange mount receptacle, shown in red for reference, connects the IF output signal to external circuitry. Four 2-56 screws secure the two block halves together. The diagonal feedhorn opening is shown at the bottom center of the Figure. A 2-56 screw tap, shown in the bottom of the block at the far right, is included for mounting the block within the cryostat cooler.
Figure 18  Shown is the AutoCAD layout of the assembled receiver block. The block consists of two halves, which are split through the middle of the reduced-height waveguide. The diagonal feedhorn is shown in the bottom center. The SMA connector is shown for reference in red.

Figure 19  Above are the AutoCAD drawings of the top half of the receiver block. The mating face, far right, shows the feedhorn leading to the microstrip channel and backshort. The IF port of the microstrip channel is connected to a quartz substrate, which sits on the recess to the left of the microstrip channel and connects to the SMA receptacle (red). All measurements are in microns.
Figures 19 and 20 show schematics of the two block halves. The microstrip channel, feedhorn terminus and backshort are located in the middle of the block, and are not visible in these two Figures due to their small size. A 250μm deep recess is located between the SMA connector and the microstrip channel. This recess accommodates a 250μm thick quartz chip with a gold microstrip patterned on top. The microstrip connects the IF beam lead of the silicon mixer chip to the SMA connector. Two aluminum pins align the block halves; the postholes for the pins are shown in the drawing of the mating faces. Two recessed volumes in the mating face of the top half of the block reduce the mating area between the two block halves.

Figure 20 Above are the AutoCAD drawings of the bottom half of the receiver block. The mating face, far right, shows the feedhorn leading to the microstrip channel and backshort. The blocks are aligned with two aluminum posts. Four 2-56 screws are used to secure the block. A 2-56 screw tap is included for external mounting. All measurements are in microns.

Figure 21 shows a close-up view of the mating face of the bottom block, which contains the microstrip channel and backshort. Also shown are the beginning of the
feedhorn (top) and the recess for the quartz IF chip (left). The silicon mixer chip is suspended within the channel by beam leads extending from the sides and ends of the chip, and is aligned such that the bowtie is co-linear with the feedhorn and backshort. The silicon mixer chip is secured in place when the two block halves are brought together, crimping the gold beam along the perimeter of the chip. The IF beam lead of the chip connects to the quartz microstrip.

Figure 21 Shown is a close-up of the mating face of the bottom half of the receiver block. Shown are the microstrip channel (vertical), the backshort (left) and the reduced-height waveguide (right). The reduced-height waveguide tapers to a full-height waveguide prior to joining up with the diagonal feedhorn. Tapering up to a full-height waveguide eases machining constraints. All measurements are in microns.

Figure 22 shows a close-up cross-section of the assembled block halves along the plane of the microstrip channel. The split plane runs through the microstrip channel and is oriented such that the top of the silicon chip is placed within the microstrip channel 39µm above the bottom of the channel. In this Figure, the recess for the quartz microstrip chip is shown to the left of the microstrip channel. The RF ground connection for the silicon mixer chip is made on the right end of the channel. A cross-section of the reduced-height waveguide is shown between the two halves of the microstrip channel.
Figure 22 A cross-section of the assembled block halves cut along the length of the microstrip channel shows the two sides of the microstrip channel, the cavity for the quartz microstrip line (left). The reduced-height waveguide intersects the microstrip channel perpendicular to the visual plane in this Figure. Note the asymmetric division of the microstrip channel. The HEB silicon chip is clamped between the two block halves. All measurements are in microns.

Figure 23 A cross-section of the assembled block halves cut along the length of the reduced-height waveguide shows the feedhorn (far right) leading to the microstrip channel and backshort. The microstrip channel is perpendicular to the visual plane in this Figure. The two block halves are split symmetrically through the feedhorn, through the E-plane. All measurements are in microns.

Figure 23 shows a close-up cross-section of the assembled block halves along the plane of the feedhorn and backshort. The microstrip channel is seen end-on in this image. The microstrip channel and backshort connect to the feedhorn through a reduced-height waveguide that flares out to a full-height waveguide before joining the feedhorn. The flare between the reduced-height and full-height waveguides is linear and expands to full-height over a length of 640 µm. The diagonal feedhorn flares out off to the right in the Figure and the backshort is seen on the left, terminating 128 µm beyond the center of
the microstrip channel. The feedhorn taper begins approximately two full wavelengths away from the mixer chip.

### 3.4 Mask Design

The fabrication of the silicon HEB mixer chip requires four photolithography masks. These are the base mask, the passivation mask, the beam leads mask and the SOI chip extents mask. The base mask consists of the low-pass filter structures and the bowtie antennas as well as adhesion pads for the beam leads. Also included with the base layer are several alignment marks around the middle of the bowtie. These are used for alignment during electron-beam writing steps. The passivation mask defines the extent of insulation over the bolometer areas. The bolometers are passivated to protect against corrosion and contamination. The beam leads mask defines the beam lead structures that extend from the sides of the silicon chips, as well as the IF and RF ground connections, which extend from the chip ends. Figures 24 through 26 show the clearfield layouts of these mask patterns, along with alignment marks.

There are three circuit patterns within the mask set, one each for 3μm, 7μm and 10μm thick silicon chips. For each of these patterns, the length of microstrip section at the ends of the bowtie antennas varies by several tens of microns. The length of the silicon chip for each pattern also varies by the same amount. Since only one third of the patterns on a given wafer correspond to the select wafer thickness, the SOI chip extents mask is designed such that only one of the three circuit patterns is released from the wafer. This is done by aligning the mask pattern shown in Figure 26 with the pattern that corresponds with the appropriate silicon chip thickness. Three sets of alignment markers are included on the base mask layer to facilitate alignment for each of the three designs.
The appropriate SOI chip pattern is selected by aligning the SOI alignment marks to the marks on the base layer that correspond to the thickness of the silicon.

**Figure 24** The base lithography mask contains patterns for the 3μm, 7μm and 10μm silicon chip designs. The base pattern consists of the IF filter structures, electron-beam alignment marks, the bowtie antenna and contact pads for the beam leads. The base pattern also contains alignment marks for aligning the insulation, plating and silicon chip masks.

**Figure 25** The plating mask defines the beam leads. Long beam leads at the end of the chip make contact to the IF output and the RF ground. The eight smaller beam leads along the side of the chip provide mechanical support for the chip within the waveguide. Three slightly different plating mask patterns were made. One, shown above, contains both the long contact beam leads and the smaller side beam leads. The other two consist of just the small beam leads or just the larger contact beam leads, allowing for the side beam leads and contact beam leads each to be a different thickness.

**Figure 26** The chip extents are defined using the above mask. Note that only one of every three patterns is exposed with this mask; this mask allows the operator to select only those patterns corresponding to the appropriate silicon thickness. The alignment marks at right are aligned with the appropriate marks shown in Figure 24, according to silicon thickness of 3μm, 7μm or 10μm.
A composite layout of the four mask layers is shown in Figure 27. This image is from the AutoCAD wire frame drawings, and shows how each of the patterns lines up with the others. Three base patterns are shown in the Figure, one each for the 3\(\mu\)m, 7\(\mu\)m and 10\(\mu\)m silicon chips. Figure 27 shows how the SOI chip pattern (blue) aligns with just one of the three base patterns (red), and the alignment marks associated with each pattern.

![Figure 27](image)

**Figure 27** Above, a composite image of the four mask patterns is shown to indicate how the patterns align with respect to one another. Wire frame models are shown to clearly show all of the patterns.

### 3.5 References


Insulating-Superconducting Receiver,” *IEEE Transactions on Microwave Theory and Technology*, 44 (9), September 1996


Chapter 4

Fabrication of Ultra-Thin Silicon Chips with Beam Leads

Superconducting devices for THz applications are often fabricated on thin quartz chips, which are then placed within the microstrip channel of a receiver. Early designs had the chips resting on the bottom of the microstrip channel. As a result, around half of the channel is occupied by quartz while the remaining volume is air. Ideally, the presence of the dielectric is minimized and the entire channel volume is of a uniform, and minimized, dielectric constant. Often, designers rest very thin chips (less than 50\(\mu\)m) along shoulders milled into the microstrip channel, thereby minimizing the volume of chip within the channel while still situating the metalized circuitry in the center of the channel [1]. However, quartz chips of these sizes may only be thinned to around 25\(\mu\)m before becoming too brittle to handle. Our work overcomes this limitation by replacing the quartz with ultra-thin silicon [2,3]. We have fabricated silicon chips that are as thin as 1.6\(\mu\)m and feature gold beam leads extending from the chip perimeter. These chips are rigid enough to be handled with a pair of fine-tipped tweezers and placed within the microstrip channel of a waveguide.

Typically, the electrical contact between the superconducting circuitry and external RF and IF connections are made via wire bonds, solder bumps, conductive gaskets or micro-springs [4,5]. Such techniques are not applicable when using silicon that is only a few microns thick, as the chip would rupture when forming these connections. To overcome this, we devised a process for making electrical and thermal contact between the chip and the waveguide block via gold beam leads. These beam
leads extend from the perimeter of the chip by up to several hundred microns and support the chip in the middle of the microstrip channel between the two halves of the receiver block.

Beam leads are often employed in RF applications, most notably in GaAs-based mixers and multipliers [6,7]. They have also been demonstrated on quartz substrates designed for superconducting SIS-based mixer applications [8,9]. Our ultra-thin silicon chips and beam leads are robust enough to handle the rigors associated with mixer assembly, even when the beam leads extended several hundred microns beyond the perimeter of the chip.

Silicon offers several material advantages over quartz for THz substrate applications, though it also has some disadvantages too. First, the rupture modulus of silicon is greater than that of quartz; 135MPa versus 50MPa. As a result, silicon may be thinned more so than quartz before it becomes too brittle to handle. The rupture modulus of a brittle material is measured using a transverse bending test in which a rod specimen is bent with a three-point loading technique. The ends of the rod are fixed while a force is applied to the center of the rod. The load at which the rod fractures, $F_f$, and the dimensions of the rod, determines the rupture modulus, $\sigma_{mr}$.

$$\sigma_{mr} = \frac{3F_fL}{2bd^2} \quad \text{Equation 1}$$

In Equation 1, $L$ is the length of the rod specimen between the two fixed points, $b$ is the rod specimen width and $d$ is the thickness. Given the rupture moduli of silicon and quartz, a silicon rod may be 60% as thick as a quartz rod of equal length and width while under an equal load at rupture, as expressed in equation 2.
Another advantage of silicon is its higher thermal conductivity, 150W/mK versus 2W/mK for quartz. On the other hand, silicon has a dielectric loss tangent that is nearly 40 times larger. However, due to the much larger thermal conductivity of silicon over quartz, the heat generated within a silicon substrate due to RF propagation dissipates rapidly. Heat flow through a solid of length L, width b, thickness d, and between two temperatures $T_1$ and $T_2$ is dictated by the material’s thermal conductivity, $K$, as shown in Equation 3.

$$Q = \frac{bd}{L} \int_{T_1}^{T_2} K dT$$

Equation 3

If the thermal conductivity is assumed to be independent of temperature, Equation 3 may be simplified.

$$Q = \frac{bd}{L} K \Delta T$$

Equation 4

In the simplified case of Equation 4, the relationship between material thickness and thermal conductivity is linear.

If the heat flowing through a silicon rod is a factor of 40 greater than the heat flow through a quartz rod (given the difference in dielectric loss tangent), and if the rod dimensions are of equal length and width, the thickness of the silicon rod could be 53% as thick as the quartz rod and maintain the same $\Delta T$ across a length L.

A second disadvantage that silicon has over quartz is its larger dielectric constant, 11.9 versus 3.8 for quartz at 10GHz. As a result, a beam of silicon looks electrically thicker to an RF signal than a quartz beam of equal physical thickness. The square root
of the ratio of the two dielectric constants determines the difference in electrical thickness, which for silicon over quartz is a factor of 1.77.

Most importantly for ultra-thin silicon chips, silicon is far more resilient than quartz. Resilience is the ability of a material to absorb energy when deformed elastically. This energy does not contribute to deformation of the material; rather, the energy is release upon unloading. Resilient materials are found in applications such as springs.

The modulus of resilience, $U_r$, is the measure of the strain energy per unit volume required to stress a material from an unloaded state to the point of yielding. Restated, the modulus of resilience is simply the area under the stress-strain curve, as stated in Equation 5.

$$ U_r = \int_0^{\varepsilon_y} \sigma d\varepsilon $$

Equation 5

Assuming a linear stress-strain curve, Equation 5 may be simplified as

$$ U_r = \frac{1}{2} \varepsilon_y \sigma_y $$

Equation 6

where $\sigma_y$ and $\varepsilon_y$ are the stress and strain at yielding, respectively. The material property $\sigma_y$ is known as the yield strength. Equation 6 may be restated using Hooke’s Law, which relates stress and strain through Young’s Modulus, $E$ (the modulus of elasticity).

$$ U_r = \frac{\sigma_y^2}{2E} $$

Equation 7

While silicon and quartz both have similar Young’s moduli (179GPa for silicon and 75GPA for quartz), the yield strength for silicon is significantly larger than that of quartz (7GPa versus 50MPa), resulting in a modulus of elasticity for silicon that is far greater than that of quartz, 450MPa versus 17kPa for quartz at room temperature [10]. Virwani
et al have shown that Young’s modulus for silicon remains unchanged between bulk measurements and measurements made from deflecting nano-scale beams [11].

The modulus of resilience represents the amount of energy a sample can absorb per unit volume before yielding. A 3μm thick silicon chip contains 16 times less volume than a 50μm quartz chip of equal width and length, but can absorb far more energy per unit volume. Ultra-thin silicon chips are therefore far less likely to rupture under applied loads during handling and receiver assembly.

We conducted numerous analytical RF studies on the feasibility of using our ultra-thin silicon chips in THz receiver applications for both single-chip receivers and array antenna structures [12]. The use of an ultra-thin silicon chip as the substrate for THz circuitry greatly simplifies the RF design process. In addition, since shoulders need not be milled within the microstrip channel to accommodate the chip, machining of the receiver block becomes much more straightforward.

4.1 Fabrication

The process for fabricating ultra-thin silicon chips with beam leads is discussed in three subsections: (i) beam lead fabrication, (ii) silicon thinning, and (iii) chip definition. In Figure 1, a process diagram outlines the fabrication steps. For this work, seven sets of silicon chips were fabricated in order to investigate variations in silicon and beam lead thickness. To simplify sample preparation, none of these chips feature submillimeter-wave circuitry such as RF filters, antennas, or active superconducting devices. When fabricating chips with such circuitry, the fabrication steps for these elements are performed between the beam lead fabrication and silicon thinning subsections [13].
A batch of ultra-thin silicon chips is defined from a square piece SOI (silicon on insulator) wafer measuring 2cm on a side. A dozen such SOI squares are diced from a larger three-inch SOI wafer, which is supplied by Soitec, Inc. An SOI wafer consists of three layers: the thick handle silicon, followed by a buried oxide layer (BOX), and then the thin device silicon. The ultra-thin chips are ultimately defined from the device silicon layer.

Figure 1 The fabrication of ultra-thin silicon chips with gold beam leads is summarized in seven steps. In (1), beam leads are fabricated atop the device silicon layer of an SOI wafer. The wafer is then mounted, beam lead side down, on to a quartz carrier (2). The handle silicon and BOX layer are then removed using a combination of mechanical lapping (3) and wet etching (4). The exposed device silicon is then patterned with thick photo resist (5), which serves as an etch mask during a reactive ion etching (RIE) process. After the RIE defines the chip extents (6), the individual chips are separated from the quartz carrier (7).
Other techniques for fabricating thin silicon chips with beam leads rely on backside lapping or wet etching to thin the silicon to within a desired thickness. Because these processes are difficult to control to within a few microns, they do not offer the thickness tolerance that is required for making chips as thin as three microns or less. The thickness of the device layer of an SOI wafer does, however, offer the necessary tolerance. By using the device silicon as our substrate, we can safely assume that the final thickness of the chip after processing is known to within 0.5μm.

4.1.1 Beam lead fabrication

Gold beam leads are electroplated atop the device silicon layer. The beam lead thickness can be varied from wafer to wafer; we have fabricated beam leads ranging in thickness from 1.0μm to 4.5μm thick. For the test wafers presented in this section, a seed layer is deposited atop the device silicon using DC magnetron sputtering in a multitarget deposition system with a base pressure of 10⁻⁸ Torr. The seed layer ensures electrical continuity across the wafer, and consists of 10nm of titanium below 50nm of gold. The titanium serves as an adhesion layer between the device silicon and the gold. An ion mill is performed for two minutes prior to titanium deposition in order to promote adhesion between the titanium and the device silicon.

The beam lead structures are defined using AZ4330 positive photoresist and an i-line contact mask aligner. Spun at 3krpm, the resist is 4μm thick, allowing for at least several a few hundred nanometers of spacing between the top of the thickest beam leads and the top of the resist. After developing the resist, a three-minute exposure to an oxygen plasma (100W, 1Torr) cleans the gold surface of any remaining organics prior to the plating process. Following resist patterning, the beam leads are plated atop the gold
seed layer with the Techniq 25E plating solution in a series of plating sequences to obtain the desired thickness. Afterwards, the resist is removed with acetone. The gold seed layer and titanium adhesion layer are removed using an iodine-based wet etch and a dilute HF-based wet etchant, respectively.

When integrating the beam lead process with either the d-HEB or p-HEB fabrication processes (Chapters 5 and 6), the beam lead fabrication steps take place after completing the definition of the bridge width RIE mask, and prior to etching the open-field HEB niobium or niobium nitride (the absorber layer). A plating seed layer is not required. Instead, the HEB absorber layer provides electrical continuity across the surface of the wafer during the plating process. After plating the beam leads and stripping the plating resist, a reactive ion etch sequence removes the open-field HEB absorber layer. Referring to the flow diagram in Figure 1, this RIE process takes place between steps 1 and 2; after plating and before mounting onto the quartz carrier wafer.

### 4.1.2 Silicon thinning

After fabricating the beam leads, we remove the handle silicon from the backside of the wafer in a two-step process. First, we thin the bulk of the handle to 30μm by mechanical lapping. Second, we use a silicon wet etch process to remove the remaining 30μm of handle silicon.

Prior to thinning, we mount the silicon wafer, beam lead side down, atop a 250μm thick quartz carrier. The quartz carrier serves as a rigid support for the wafer, which loses most of its mechanical rigidity after the handle silicon has been removed. A clear mounting wax (Stronghold 7036) adheres the wafer to the carrier. The quartz
carrier and clear mounting wax allow for a subsequent backside alignment process, which is necessary for aligning the chip extents with respect to the beam leads.

Next, the wafer/carrier pair is mounted atop a thick metal lapping block using the same clear wax. A mechanical pressure jig then planarizes the wafer and carrier with respect to the lapping block [14]. With the wafer, carrier and lapping block inside, the jig is heated to an internal temperature of 120°C, which causes the wax to melt. Pressure (10psi) is uniformly applied to the wafer via a silicon membrane within the jig for 20 minutes. The jig is then cooled to solidify the planarized wafer and carrier atop the lapping block. After cooling, the pressure is released and the wafer is ready for the first step of the thinning process.

A mechanical lapping process removes the majority of the handle silicon. Our lapping system consists of a Techprep Polishing Machine and a Multiprep Positioning Device, both made by Allied High Tech Products, Inc. A 30μm grit diamond lapping film reduces the handle silicon to within 30μm +/- 5μm of the BOX layer. Lapping requires approximately an hour to complete. Afterwards, the carrier and wafer are removed from the lapping block.

A wet etch solution removes the remaining handle silicon. The etchant consists of TMAH (tetramethyl ammonium hydroxide, (CH₃)₄NOH), diluted to 8% by weight in de-ionized water, and heated to 60°C +/- 3°C [15]. The BOX layer serves as an etch stop; the high selectivity of the TMAH etchant between silicon and silicon dioxide ensures that the BOX layer protects the underlying device silicon from the heated etchant.

In order to prevent the etchant from seeping under the wafer and attacking the device silicon, the wafer and carrier are placed in a jig that prevents the etchant from
contacting the wafer sides. The clear mounting wax is highly susceptible to the TMAH etchant, especially at elevated temperatures. If the wax is exposed to the etchant, etchant will seep under the wafer and damage the device silicon. The jig prevents contact between the etchant and the device silicon by sealing the wafer along its perimeter with a silicone rubber gasket. A CAD drawing of the etch jig is shown in Figure 2. An o-ring seals the outer perimeter of the jig from the etchant by forming a seal between the upper and lower jig plates. A thin sheet of silicone rubber between the upper jig plate and the top side of the wafer seals the inner perimeter of the jig.

**Figure 2** A cross-sectional CAD drawing shows the wet etch jig. The jig protects the perimeter of the wafer from attack by the heated TMAH etchant. A clear wax used to adhere the wafer to the quartz carrier is susceptible to the etchant and, if attacked, would allow etchant to attack the device silicon. The wafer (green) sits upside-down atop a quartz carrier (light blue) and is exposed to the etchant through the hole in the jig (blue). When the two halves of the jig are pressed together, an o-ring and a silicone gasket (red) are compressed, preventing the etchant from attacking the wafer perimeter.

A peristaltic pump re-circulates fresh etchant to the etch surface. Due to the uncertainty in the handle thickness after mechanical lapping, etch times range from 3 to 4.5 hours. The etch rate depends significantly upon temperature, and increases considerably with increasing etchant temperature [16,17]. However, the etchant is maintained at a temperature no higher than 60°C because the clear mounting wax will soften and re-flow at temperatures beyond 70°C. When the handle silicon is etched to within a few microns of the BOX layer, the membrane becomes extremely delicate. At this stage, the thin film may crack and peel if perturbed by flowing wax. At 60°C, the wax
does not free-flow, yet the etchant is heated sufficiently to maintain a reasonable etch rate.

The etch progress may be monitored by paying attention to the etch surface during the course of the process. When etching the bulk of the handle silicon, the etch surface has a characteristic silicon-grey color. As the etch proceeds towards the BOX layer, the handle silicon becomes pinkish. As the pinkish handle material dissolves, the BOX layer becomes visible, which has a characteristic metallic green color. The etch process may be terminated once the BOX layer is completely free of the pinkish handle silicon.

### 4.1.3 Chip Definition

After removing the handle silicon, an etch mask is patterned with photoresist on the backside of the wafer in preparation for reactive ion etching of the device silicon. The photoresist etch mask defines the individual chip extents, so it must withstand the high energy ion bombardment and chemical attack associated with the reactive ion etch of the device silicon.

The reactive ion etch conditions are 11.7sccm of CCl$_2$F$_2$, 13.5sccm of SF$_6$, 7sccm of argon, 30mT pressure and 0.3W/cm$^2$ RF power. Etching of silicon with this chemistry is discussed in detail by Rangelow et al [18]. For the same reasons discussed in association with the TMAH etch of the handle silicon, the etch conditions in the RIE chamber are controlled to prevent the wafer from heating beyond the melting point of the mounting wax. To prevent excess heating, the platter of the RIE is cooled to 8°C. In addition, the RF power is cycled such that it is on for one minute and then off for two minutes, allowing the sample to cool after each brief etching sequence. As a result of
cooling, however, the etch rate of the device silicon decreases considerably compared to the results presented by Rangelow; the etch rate of the device silicon is 126 nm/min with a standard deviation of 3 nm/min when using a photoresist mask.

Two masking methods were developed for the reactive ion etch of the device silicon. Both of these are designed to withstand the conditions associated with removing several microns of silicon in the Rangelow etch. The first masking method takes advantage of the BOX layer present atop the device silicon. In this process, the BOX layer is completely removed during the RIE step. For the Rangelow chemistry, silicon dioxide etches approximately one third as fast as silicon. Therefore, using a 1 µm BOX layer mask results in a chip thickness of 3 µm, so long as the original device silicon thickness is greater than or equal to 3 µm and the etch is terminated immediately after the silicon is fully removed. A backside photolithography process defines a layer of AZ5214 photoresist atop the BOX. Exposure to an HF-based wet etchant removes the exposed BOX layer. The resist is then dissolved in AZ400K developer (undiluted), leaving behind the patterned BOX layer.

The second masking method does not rely on the BOX layer, which instead is removed by an HF-based wet etchant prior to photoresist patterning. In order to withstand the RIE conditions, a photoresist mask several microns thick is patterned on the exposed device silicon. For this work, we used both AZ4330 and AZ4620 photoresists. Both resists withstand the extended etch periods and energetic etch conditions associated with the Rangelow etch. After spinning, the AZ4330 is 4 µm thick, which is sufficient for masking device silicon that is 3 µm thick or less. For thicker device silicon, the AZ4620 is used, which is spun on to a thickness of 7 µm. These resists etch at a rate of around
80nm/min in the Rangelow chemistry. Figure 3 shows two optical images of wafers patterned with photoresist. The top image is a bright-field photograph showing the photoresist pattern atop the device silicon. The lower image is back-lit, and shows the alignment of the photoresist patterns with respect to the beam leads on the opposite side of the wafer. After the etch, a combination of O₂ plasma etching and exposure to undiluted AZ400K removes the remaining photoresist. Figure 4 shows two completed chips still attached by wax to the carrier wafer.

**Figure 3** Shown are two photographs taken after patterning of the photoresist mask. The top half of the Figure is a bright-field photograph showing the photoresist pattern atop the device silicon. The bottom half of the Figure was taken while illuminating the same region from the backside of the wafer. Since the device silicon is translucent and the gold beam leads are opaque, the alignment of the photoresist on the top of the wafer with respect to the beam leads on the underside of the wafer is observed. The photoresist pattern is 800μm long.
Figure 4  Shown are two completed chips after the reactive ion etch of the device silicon and removal of the masking photoresist. The back sides of the chips are shown since the wafer was flipped upside-down prior to etching. The chips are still attached to the quartz carrier by the clear mounting wax. The gold beam leads are clearly shown, extending from the perimeter of the chips. The smaller beam leads along the length of the chips will serve as mechanical supports, allowing the chip to be suspended within the microstrip channel of the receiver block. The two longer beam leads provide IF and RF ground connections to the circuitry on the topside of the chips. The silicon chips are 800μm long.

Etching results using these two masking processes are different in a number of notable ways. First, the wet etch of the BOX masking pattern results in a rough etch mask perimeter. These errors transfer to the device silicon during the RIE, resulting in rough chip perimeters. Another problem associated with the BOX method is lateral under-etching of the device silicon during the RIE process. Lateral under-etching is prevented in the photoresist process by sidewall deposition of fluorinated polymers. The polymeric photoresist disassociates during the RIE process, allowing for polymerization of hydrogen, carbon, and fluorine along the sidewalls of the etched silicon [19]. The sidewall polymerizations prevents chemical attack of the silicon, thereby preventing the etching of silicon directly underneath the photoresist mask. A third difference between the two masking processes is shown graphically in Figure 5. The BOX-based process results in a 200nm standard deviation in final chip thickness. In contrast, the photoresist
masks produce a standard deviation of no more than 50nm for a given wafer. The difference is associated with the rapid etching of the BOX mask and the variations in etch rate across a wafer. It takes on average three minutes for an entire chip to etch through to the carrier wafer after the first part of the wafer shows evidence of being complete. This variation in etch rate results in variations in final chip thickness since the BOX masking patterns etch away prior to completion of the etch. The chips masked with photoresist do not demonstrate such large variation in thickness since several microns of photoresist remain atop the device silicon after the etching is complete.

![Figure 5](image-url)  

**Figure 5** Etch time versus silicon thickness is dependant upon the type of mask used during reactive ion etching. Photoresist masks are more durable, and do not degrade significantly during the etch process. As a result, the distribution of chip thickness is small, around 50nm. Etching with a BOX mask leads to greater distribution in the final chip thickness due to rapid depletion of the BOX layer; standard deviation is around 200nm.

After etching, the individual chips are removed from the quartz carrier by rinsing in acetone, which dissolves the mounting wax. The chips separate from the carrier and float free within the acetone-filled beaker. The chips are then collected by slowly pouring the acetone through filter paper. A light rinse with methanol removes any remaining organic debris atop the chips.
4.2 Discussion

Seven batches of silicon chips, with thickness ranging from 1.6μm to 4μm, were fabricated for this work. Table 1 lists a summary of specifications for these wafer samples and Figure 6 shows a completed silicon chip with beam leads. Chip yields exceed 90%. With the exception of one batch, the silicon chips from each batch measure 76μm by 800μm; the chips from batch 30508S measure 500nm by 2mm. In all cases, the chips are durable and can withstand the rigors of receiver block assembly. None of the samples are too brittle to handle; the largest chips from batch 30508S were also the thinnest, measuring just 1.6μm thick.

Figure 6 The above ultra-thin silicon chip features beam leads extending from the sides and ends of the chip, the longest of which extend 250μm beyond the perimeter. The silicon chip and the gold beam leads are both 2.7μm thick.

The gold beam leads adhere very well to the silicon chips; none of the chips from the seven batched listed in Table 1 are missing any beam leads. The successful adhesion is attributed to the 10nm thick titanium adhesion layer that is deposited prior to the seed
layer gold. Figure 7 shows two SEM micrographs of completed beam lead chips. The micrographs show the profiles of several ultra-thin silicon chips with gold beam leads.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Beam Lead Thickness</th>
<th>Silicon Thickness</th>
<th>RIE Mask Type</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>30508S</td>
<td>4.5μm</td>
<td>1.6μm +/- 30nm</td>
<td>Photoresist</td>
<td>Chip length 2mm</td>
</tr>
<tr>
<td>30625SB</td>
<td>1.5μm</td>
<td>3.0μm +/- 203nm</td>
<td>BOX</td>
<td>Large variation Si thickness</td>
</tr>
<tr>
<td>30625SD</td>
<td>2.7μm</td>
<td>2.7μm +/- 32nm</td>
<td>BOX</td>
<td>10% over-etch of Si</td>
</tr>
<tr>
<td>30702SA</td>
<td>1.9μm</td>
<td>3.0μm +/- 34nm</td>
<td>Photoresist</td>
<td></td>
</tr>
<tr>
<td>30702SB</td>
<td>1.1μm</td>
<td>3.3μm +/- 54nm</td>
<td>Photoresist</td>
<td></td>
</tr>
<tr>
<td>30702SD</td>
<td>0.2μm</td>
<td>3.3μm +/- 13nm</td>
<td>Photoresist</td>
<td>Beam leads too thin</td>
</tr>
<tr>
<td>30714SB</td>
<td>1.5μm</td>
<td>4.0μm +/- 16nm</td>
<td>Photoresist</td>
<td>BOX was 1.5μm thick</td>
</tr>
</tbody>
</table>

Table 1: Shown is a summary of the wafer batches that were fabricated during the development of the SOI beam lead process. Silicon thickness ranges from 1.6μm to 4μm while beam lead thickness ranges from 1.1μm to 4.5μm.

All of the samples presented in this work feature thick gold beam leads extending from the perimeter of the silicon chips. Functional beam lead thickness ranges from 1μm to 5μm thick and the beam leads extend up to 260μm beyond the perimeter of the chip. The 200nm thick beam leads of batch 30702SD were too thin to maintain shape. The 200nm beam leads behave like a foil, and lack the springiness associated with the thicker beam leads. It may be possible to fabricate beam leads as thin as 200nm by substituting sputtered or evaporated gold for the plated gold.

Figure 7: The left micrograph shows a 4μm thick silicon chip with 1.5μm thick gold beam leads of various lengths protruding from the perimeters. The longest beam lead extends 260μm beyond the edge of the silicon. The right image shows a 1.6μm thick chip with a 4.5μm thick beam lead.
As an initial demonstration of the durability of the beam leads and the ultra-thin silicon chips, we placed the chips within a 100nm wide microchannel and compressed the beam leads along the channel shoulder. The microchannel was diced within a silicon wafer using a wafer-dicing saw. The beam lead chips were positioned within the microchannel, which was defined within a silicon wafer using a dicing saw. A glass slide was then placed on top of the microchannel, and then clamped down to simulate the force associated with the clamping of two receiver block halves. Using the glass plate to simulate the upper block half allowed the beam leads to be observed as pressure was applied. The beam leads, 1.5μm thick in this case, supported the chip through the experiment and did not tear of break away from the silicon chip. Figure 8 shows a photograph of a chip in the microstrip channel. Pressure applied to the glass slide creates the multi-colored interference rings that are seen atop the gold beam leads.

**Figure 8** A 4μm thick silicon chip with 1.5μm thick gold beam leads rests within a microstrip channel. A glass slide is clamped over top of the sample in order to simulate the pressure associated with compressing the beam leads between the two halves of a receiver block. The glass slide allows the gold beam leads to be observed as pressure is applied. The interference rings seen atop the gold beam leads are created when the glass slide contacts the beam leads.

### 4.3 Conclusion

We developed a process for fabricating ultra-thin silicon chips with gold beam leads and demonstrated the process by fabricating chips with silicon thickness of 1.6μm, 3μm and 4μm. These chips feature beam leads that range in thickness between 1μm and 4.5μm. Mechanically, the beam leads are sufficiently rigid to handle with tweezers and compress between receiver block-halves.
RF simulations show that such chips are useful for superconducting SIS and HEB THz receiver applications. In addition, incorporating these chips into THz superconducting receivers greatly simplifies receiver design, block machining and receiver assembly. Superconducting circuits with beam lead RF and IF connections ease the assembly of receivers since the electrical connections to the chip do no require wire bonding, soldering or connection via gaskets or micro-spring contacts. Beam lead connections facilitate the rapid replacement of individual receiver components, and allow non-functioning elements to be discarded without having to replace entire arrays.

4.4 References


Chapter 5

Fabrication of Diffusion-Cooled Hot-Electron Bolometers

Research on novel devices for heterodyne mixing, such as hot-electron bolometers, aims to extend experimental capabilities of receivers into the THz frequency domain. Hot-electron bolometers come in two varieties, both of which we fabricate at the University of Virginia. The first of these is the phonon-cooled bolometer (p-HEB), which was proposed by Gershenzon et al in 1990 [1,2]. The p-HEB device relies on electron-phonon interactions as the dominant cooling mechanism for the bolometer. We discuss in detail the fabrication of p-HEBs in Chapter 7. In 1993, Prober proposed a second type of hot-electron bolometer, one that employs rapid electron diffusion as the dominant cooling mechanism [3]. These devices are known as diffusion-cooled HEBs (d-HEBs), and are much more narrow than p-HEBs. The d-HEBs consist of a thin superconducting film contacted on either end by thick gold cooling pads. The cooling pads serve as heat sinks, which ensure that the outflow of electrons dominates the thermal conductance of the bolometer over the slower electron-phonon interactions.

5.1 d-HEB Fabrication

We fabricate d-HEBs on both fused quartz and silicon-on-insulator (SOI) substrates [4-6]. The discussion of the fabrication process consists of five parts: (i) the deposition of the HEB niobium (ii) fabrication of the HEB cooling pads (defining the HEB bridge length) (iii) definition of the HEB bridge etch mask (iv) the etch of the HEB bridge, and (v) passivation. Figure 1 outlines some of the steps of the d-HEB fabrication process.
Figure 1 A schematic outline of the UVa EBL HEB fabrication process is shown above. A top down perspective, shown in the left-most column, is complimented by cross-sections along the x-axis (center column) and the y-axis (right column). EBL lift-of processes are used to define the nanometer dimensions of the d-HEBs, and are shown schematically in steps 2 and 3. After patterning the gold/nobium masking layer above the HEB bridge location, a three part reactive ion etch process is used to define the niobium bridge (steps 4 through 6). After defining the microbridge, the devices are passivated by patterning a large square of germanium atop the junction area (not shown).
5.1.1 HEB Niobium Deposition

The HEB niobium is a 10nm to 15nm thick film, from which the bolometer bridge is defined. The HEB niobium thickness is adjusted to achieve a desired sheet resistance; within the 10nm to 15nm thick range, the sheet resistance varies from 35 to 20 ohms per square (written as Ω/□). Given this sheet resistance, the normal-state resistance of the bolometer (usually 35Ω to 50Ω at 4K) is defined by using only a few series squares of material. Minimizing the number of squares needed to achieve the required device resistance minimizes the bridge length, thereby allowing electrons to diffuse quickly into the cooling pads during RF operation.

On top of the HEB niobium, we deposit a thin over-layer of gold. The gold over-layer prevents the HEB niobium from oxidizing during subsequent fabrication processes, thereby promoting better electrical continuity between metal layers and preventing contamination of the HEB niobium layer. Typically, the over-layer gold is 10nm thick, which is enough to ensure that the HEB niobium does not oxidize during the subsequent fabrication processes.

Both layers are deposited without breaking vacuum using DC magnetron sputtering. Our multitarget sputtering system features four sputtering guns and an ion miller, and has a base pressure of 10^{-8} Torr. Deposition conditions for the niobium are controlled in order to achieve a zero-stress thin film. A zero-stress condition optimizes the superconducting properties of the niobium film. To achieve zero-stress niobium, a light ion mill is performed prior to deposition in order to drive off excess absorbed moisture from the substrate surface [7]. Gun bias conditions also affect film stress. Bias conditions include sputter pressure (controlled with argon) and either gun power, voltage
or current. These conditions are monitored and adjusted as the niobium target erodes with long-term use [8]. Techniques for mounting wafers on deposition blocks also influence niobium stress. Efforts to implement stress-minimizing float-block mounting schema were not used with SOI wafers due to the small size of the substrates (around 2cm or less), and the higher rigidity of the 350μm thick SOI chips with respect to our 250μm thick quartz substrates [9].

After depositing the HEB niobium and gold over-layer, the micron-scale features of the wafer, such as RF filters and bowtie antennae, are fabricated using standard optical lithography. These patterns consist of a layer of thick gold (typically 200nm). The gold is evaporated in a multi-source electron-beam evaporation system, which has a base pressure of $10^{-7}$ Torr. In order to promote adhesion between the evaporated gold and the over-layer gold, a thin (10nm) layer of titanium is first evaporated. After evaporation, lift-off is performed in a one-to-one solution of NMP (N-methyl-2-pyrolidinone) and propylene glycol heated to 120C. Patterned along with the RF structures and near the bowtie antennae are sets of small alignment marks. In subsequent processing steps, NPGS uses these marks to precisely pattern the gold cooling pads and microbridge patterns in a layer of poly(methyl methacrylate) (PMMA).

### 5.1.2 Cooling Pad Definition

Once the alignment marks are in place, a bilayer of electron-beam sensitive resist is spun atop the wafer. This bilayer consists of a low molecular weight (MW) layer of PMMA below a high MW layer of PMMA. The high MW PMMA (950kg/mol) maximizes pattern resolution. The low MW PMMA (495kg/mol), which solves more readily due to its shorter polymeric chains, provides an undercut beneath the high MW
PMMA after developing. This undercut prevents metal sidewall deposition from forming a continuous vertical structure along the pattern perimeter. As a result, the lift-off solution may more easily solve the PMMA, thereby facilitating lift-off. Importantly, the stepped profile allows for a smooth pattern edge by preventing vertical sidewall metal from adhering to the pattern perimeter. Such sidewall material often folds over, causing shorts across the HEB gap. Figure 2 outlines the bilayer fabrication process, and the subsequent metal deposition and lift-off. The Figure also shows an optical image of a bilayer resist pattern that clearly demonstrates the undercut.

![Figure 2](image.png)

**Figure 2** The bi-layer resist structure facilitates lift-off by limiting sidewall deposition. A low molecular weight PMMA (495kg/mol) and a high molecular weight PMMA (950kg/mol) are spun over a sample, with the low molecular weight PMMA on the bottom (A). Upon exposure to the electron beam, both polymers experience chain scission. Exposure to the developer solves the low molecular weight polymer chains in both layers. Since the bottom layer PMMA has a higher density of low molecular weight polymeric chains, the developer undercut the upper, high molecular weight, PMMA layer. This results in a stepped resist profile (B). Isotropic components of the subsequent metal deposition process result in a thin metal layer depositing along the sidewalls of the resist (C). Due to the undercut profile though, there is a discontinuity in the material deposited along the pattern sidewall. Therefore, the resist structure remains susceptible to the lift-off solvent. The upper layer PMMA defines the dimensions of the deposited metal (D). The rightmost optical image shows a pattern written in a bi-layer structure (E). Magnification is 2000X, and the minimum pattern width is 4μm. Since the top layer PMMA is translucent, the absence of the bottom layer PMMA is visible (orange in absence). The undercut is approximately 600nm. In this case, the bottom layer is a 50kg/mol molecular weight P(MMA,MAA) copolymer, which increases the undercut and makes it more visible than it otherwise would be with a 495kg/mol PMMA.
Two PMMA solutions, 495 A2 and 950 A2, are successively spun at 1.0krpm and 1.5krpm, respectively, for 45 seconds. After spinning each layer, the resists cure by baking at 120C for five minutes. The resulting bilayer resist structure is around 200nm thick.

After building the PMMA bilayer, the gold cooling pad patterns are aligned and then written using NPGS using an exposure dose of 200μC/cm². Patterns develop in a two-minute rinse consisting of methyl isobutyl ketone (MIBK) and isopropyl alcohol (IPA) in a 1 to 3 ratio. Developing is followed by a 30 second rinse in IPA, which rinses the wafer surface of developer and removes any remaining surface scum.

Once exposed and developed, several layers of gold and titanium are evaporated atop the wafer. Using an evaporation process rather than a sputtering process to deposit these metals significantly reduces the occurrence of sidewall deposition along the patterns in the PMMA. Despite the use of a bilayer PMMA process, sidewall deposition was seen to frequently occur when using sputtering systems to deposit the metal for the cooling pads. Even though some wafers showed yields of up to 93% for this step, yields as low as 27% occurred just as often. Since adopting the evaporation process, yields are consistently greater than 95%.

The layers deposited during this step are, in order of deposition, 10nm of titanium, 50nm of gold, followed by another 10nm of titanium. The first layer of titanium promotes adhesion between the over-layer gold and the 50nm gold layer. The 50nm gold layer provides the thermal heat sink at the ends of the bolometer microbridge. The second titanium layer protects the cooling pad gold during a reactive ion etch of the over-layer gold.
The first five wafers that were fabricated during the development of this process showed very large standard deviations in the gold pad spacing. Upon analysis, this deviation was attributed to how often the electron beam was focused during the writing process. For these first five wafers, the beam was focused in close proximity to a writing location, the pattern was written, and then the stage was moved 900μm to align the second writing location. Prior to writing at the second location however, the beam was not re-focused. As a result, a histogram plot of the gold pad spacing for a given wafer shows a two-peaked distribution. One peak corresponds to the patterns written immediately after focusing, while the second peak corresponds to the devices written without having focused prior to writing. The red bars (wafer 31023D1) in Figure 3 show just such a distribution. The standard deviation of the gold pad spacing for the red data set in the Figure is 20nm. By focusing the beam prior to writing at every one of the device locations, the standard deviation decreases by more than 15nm. The standard deviation of the second data set in Figure 3 (wafer 31226D1, blue) is 4.4nm.

The gold patterns are complete following lift-off in trichloroethylene (TCE) heated to 70C. Lift-off takes around 15 minutes to complete, and is facilitated by occasional in-situ surface agitation by spraying with TCE and wiping the surface with a cleanroom-style wiper. The SEM micrograph in Figure 4 shows a pair of completed gold pads.
Figure 3 The above histogram plots demonstrate the improvement in the distribution of gold pad pattern spacing. Prior to pattern writing, the electron beam was focused at every other pattern location on wafer 31023D1, giving rise to the two-peaked distribution (red). For wafer 31226D1 (blue), the gold pad patterns were written after focusing the electron beam prior to every writing step. The standard deviation of gold pad spacing is 19.9nm for wafer 31023D1; the deviation is 4.4nm for wafer 31226D1.

Figure 4 The above micrograph shows a set of completed cooling pads. The tops of the gold pads are covered with titanium, which appears darker than the surrounding HEB gold/niobium bilayer. The average pad spacing from this batch (31023D4) is 275nm.

On a final note, the cooling pads are written by NPGS according to the dimensions of a pattern in a DesignCAD file. However, the spacing of the gold pads as
they are measured in an SEM does not correspond with the spacing as it is defined in the CAD file. A likely cause is an incomplete curing of the PMMA resist layers. Typically, PMMA is cured at 160C or higher for as long as 15 minutes or more. Curing promotes cross-linking of PMMA chains, which further reduces the resist sensitivity to the developer. However, out of concern for damaging the HEB niobium thin film, we do not subject our HEB wafers to processing temperatures in excess of 120C. As a result, our PMMA is probably not fully cured. The partially cured PMMA is slightly more solvable in the developer solution, and therefore, the patterns are wider than desired. Figure 5 shows the relationship between the actual microbridge length versus the CAD pattern spacing.

Figure 5 The bridge length of an HEB is determined by a pattern written in DesignCAD. NPGS reads this pattern and writes the electron beam accordingly. However, the actual bridge length turns out to be shorter than the CAD pattern spacing, so it is necessary to compensate for the difference. The above chart is used to determine the CAD pattern spacing that is required to achieve a desired bridge length. Exposure dose for all cases is 200μC/cm².

5.1.3 Niobium Mask Definition

After lift-off, a second NPGS process defines the niobium microbridge. For this step, a single PMMA layer, 950 A4, is spun over the wafer at 2krpm for 45 seconds,
resulting in a PMMA thickness of around 300nm. After alignment, a pattern is exposed above the gold cooling pads that is as wide as the desired niobium microbridge. The pattern used to define the niobium strip consists of three parts; the pattern looks much like a dumbbell, with two large pads on the ends connected by a thin line between them. The end pads serve as visualization markers, allowing the operator to inspect the patterns optically after developing. The thin line between the dumbbell ends is too thin to evaluate using an optical microscope.

The thin line between the dumbbell ends is defined in NPGS as a line dose, which consists of a single linear series of exposure points. The spacing between the points is called the center-to-center spacing, and each point is exposed for a time period known as the dwell time. Variations in the center-to-center spacing and the dwell time result in variations in line dose, which in turn affects the line width.

Using a single line to define the niobium masking strip allows for greater control than when using an area pattern. NPGS converts a CAD pattern area to a series of lines. For pattern dimensions on the order of the beam spot size, NPGS interprets an area as a series of lines. This can lead to errors in the exposed pattern, so it is best to define the niobium masking strip as a single line within the DesignCAD file. By calibrating how the line width changes as a function of center-to-center spacing and dwell time (i.e. line dose), the linewidth is accurately controlled by the operator. The error associated with defining the pattern as an area in DesignCAD is shown in Figure 6. As shown, there is significant variation between the DesignCAD pattern area line width and the actual pattern width. The Figure plots the difference between the CAD pattern and the larger, measured pattern as a function of CAD pattern width and EBL area dose. In general,
there is a decrease in pattern deviation as the CAD pattern width decreases, however, the change is neither linear nor consistent. Figure 6 also shows the affect of area dose on pattern width. Between 240μC/cm² and 280μC/cm², the pattern width does not vary significantly as a function of area dose. The patterns measured for Figure 6 were measured after depositing 20nm of gold and 20nm of niobium within the developed PMMA pattern.

![Image](image.png)

**Figure 6** Using pattern files that are drawn in DesignCAD and then interpreted by NPGS results in an unpredictable relationship between the CAD pattern width and the actual pattern width that is exposed by the electron beam. The above graph plots the CAD pattern width versus the deviation from that width as measured using an SEM. The relationship does not show a predictable pattern and so cannot be used to define the nano-scale linewidths needed for the HEB bridge width.

In contrast to Figure 6, Figures 7 and 8 show a repeatable relationship between line pattern width and dwell time for a pattern defined as a line rather than an area. Figure 7 shows a scatter plot of linewidth patterns written at several locations on four test wafers. In order to determine a predictable relationship between the line width and the line dose, the average line width and standard deviation were calculated for a multitude of line doses. Averages were only calculated when ten or more data points were available per line dose point. A second order polynomial fit was then applied to the
averaged data. The averaged data points are shown in Figure 8 along with the fitted curve. This second order equation determines the required line dose for a desired line width. The maximum standard deviation for the averaged points is 5.4nm. A minimum linewidth of roughly 80nm is possible when using this method.

**Figure 7** Shown is a scatter plot of linewidth patterns written at several locations on four test wafers. These data sets were used to calibrate the average linewidth as a function of line dose. The averaged data points were fitted with a second order polynomial trend line, as shown below in Figure 8. A double-pass method was used to write the lines measured for this data. The line dose in the x-axis of the Figure is for a single pass.

**Figure 8** Shown are the averaged line widths as a function of line dose. A second-order polynomial is fitted to the locus of points. This polynomial relates the required line dose to a desired HEB microbridge width. A double-pass method was used to write the lines measured for this data. The line doses along the x-axis in the Figure are for a single pass.
A double-pass method is used to write the line patterns between the cooling pads. The double-pass method involves writing the same pattern twice over, with a minimal delay between the two writing sweeps. The line dose is split between the two passes, so that half the dose is delivered during each pass. By using the double-pass method, the width of the line seems to be more uniform along the length of the line in contrast to when the entire dose is delivered in a single pass.

After writing and developing the line patterns above the bolometer locations, 20nm of gold followed by 20nm of niobium are sputtered over the wafer. Following lift-off in heated TCE, a thin metal pattern remains, spanning the gold cooling pads. This metal pattern serves as a mask during a series of reactive ion etches, which define the niobium microbridge. Figure 9 shows an SEM micrograph of a microbridge mask pattern.

![Figure 9](image.png)

**Figure 9** The above SEM micrograph shows a microbridge etch mask spanning two cooling pads. The mask protects the underlying HEB niobium during a reactive ion etch process. The bridge widths from this wafer (31104D1) are around 130nm. The average length-to-width ratio for the batch is 1.96, with a standard deviation of 0.073.
Prior to writing the patterns for the microbridge masks, the cooling pad spacing for every device on a wafer is measured in an SEM. When writing the microbridge mask patterns, the linewidth of the pattern is calculated to achieve the desired length-to-width (L/W) ratio. The L/W target is always the same for all of the devices in a batch, and is typically equal to 2 in order to achieve a device resistance of 35Ω at 4K (70Ω at room temperature). Even though the cooling pad spacing for every device on a wafer is intended to be the same length, there is a deviation associated with the cooling pad spacing, as discussed previously and shown in Figure 3. By tailoring the linewidth for every individual device on a wafer according to the cooling pad spacing of each device, the deviation of the L/W ratio is dependant only on the deviation of the linewidth, and not the cooling pad spacing. Therefore, the L/W standard deviation for a batch of devices is greatly reduced. Typically, a standard deviation of 5nm or less is associated with the linewidth dimension, and the resulting deviation of the L/W ratio is around 0.07 for a L/W ratio target of 2.

Figure 10 shows a set of average linewidth data points as a function of line dose. Superimposed against the data points is the second-order curve fit that was used to determine the required line dose for each linewidth. The data points are from wafer 31226D1, which contains 74 devices. As shown, there is a distribution of linewidth targets, which is due to the deviation in cooling pad spacing. The target linewidths range from 114nm to 123nm. This method yielded a maximum standard deviation for the microstrip mask linewidths on wafer 31226D1 of only 5nm.
The average linewidth as a function of line dose is shown for the microstrip masking patterns of wafer 31226D1, which contained 74 devices. The maximum standard deviation of linewidth is 5nm. Superimposed against the average linewidth data is the second-order curve fit that was used to determine the required line dose for a given linewidth.

5.1.4 Microbridge Etching

The multi-step reactive ion etch (RIE) of the microbridge consists of three parts. First, an argon-based physical etch removes the open-field over-layer gold, exposing the HEB niobium everywhere except under the niobium bridge mask. Etch conditions are: argon 67sccm, 30mT pressure, and 140mW/cm² RF power density. Next, and without breaking vacuum, an SF₆-based etch (SF₆ 13.5sccm, CHF₃ 10.6sccm, N₂ 1.6sccm, 30mT pressure, and 110mW/cm² RF power density) removes the exposed open-field HEB niobium, thereby defining the width of bolometer microbridge. This SF₆ etch also removes the niobium microbridge mask layer. The remaining gold atop the microbridge, which includes the masking gold and the over-layer gold, is then removed using a second argon-based etch process, identical in conditions to the first. Figure 11 shows an SEM micrograph of a completed d-HEB microbridge on a silicon substrate.
5.1.4 Passivation

Immediately after defining the HEB bridge in the reactive ion etcher, the wafer is transferred to the evaporator system where a layer of germanium is deposited atop the devices. By covering the niobium bridges with a layer of germanium, the bolometers are sealed off from potential contamination and additional oxidation, both of which can cause the bridge to become an open circuit. Though it is a semiconductor, at terahertz frequencies germanium behaves as an insulator, and so does not short the bolometer junction during RF operation.

After evaporating 300nm of germanium, the wafer is patterned using standard photolithography to define square patterns of photoresist atop the junction areas. The photoresist patterns serve as etch masks during a subsequent SF$_6$-based reactive ion etch of the unprotected germanium. Etch conditions are identical to the reactive ion etch recipe that is used to etch the HEB niobium. The etch process requires around 60
seconds to completely remove the open-field germanium. Afterwards, the photoresist is left atop the germanium patterns.

5.2 Results

Because the RIE mask consists of niobium and gold, an additional ex-situ fabrication step is not required to remove the masking layers after the niobium microbridge is defined. The niobium part of the mask is removed during the SF₆-based RIE of the HEB niobium, and the remaining gold is removed with a brief, in-situ, argon etch. Other EBL-based schema for HEB fabrication employ masking materials such as aluminum, PMMA or a negative-tone resist, all of which must be removed after defining the microbridge. By designing the RIE process to remove the niobium masking layer concurrently with the HEB niobium, and then the gold over-layer immediately afterward, additional fabrications steps are not required while the fully-defined microbridge is sensitive to electrostatic discharge and oxidation.

The distribution of bridge resistances for a given batch of d-HEBs is larger than the distribution of the bridge length-to-width ratio. The data presented in Table 1 show a range of resistances from a batch of d-HEBs. Each of these devices was etched separately, and then measured immediately after being removed from the RIE vacuum chamber. The average bridge resistance is 61Ω, 9Ω smaller than the 70Ω room temperature target resistance (35Ω at 4K). Bridge lengths for this batch are on average 229nm long, with a standard deviation of 2.7nm. The batch L/W ratio average is 1.96 and has a standard deviation of 0.03. Given this L/W ratio and the average batch resistance, the calculated sheet resistance of the 10nm thick HEB niobium film is 31.1Ω/□, or 3.9Ω/□ less than the expected sheet resistance. The L/W standard deviation
suggests that the distribution of resistances for this batch should then be around 1Ω, which is clearly not the case. Instead, the distribution of the data presented in Table 1 is around 10Ω, suggesting that other processing factors play an important role in determining bridge resistance besides the L/W ratio of the etch mask.

<table>
<thead>
<tr>
<th>Device #</th>
<th>Resistance</th>
<th>$SF_6$ Etch Time (sec)</th>
<th>2nd Argon Etch Time (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>59Ω</td>
<td>30</td>
<td>1.5</td>
</tr>
<tr>
<td>4</td>
<td>54Ω</td>
<td>30</td>
<td>1.5</td>
</tr>
<tr>
<td>7</td>
<td>51Ω</td>
<td>30</td>
<td>1.5</td>
</tr>
<tr>
<td>8</td>
<td>54Ω</td>
<td>30</td>
<td>1.5</td>
</tr>
<tr>
<td>9</td>
<td>76Ω</td>
<td>30</td>
<td>1.5</td>
</tr>
<tr>
<td>10</td>
<td>70Ω</td>
<td>30</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Table 1: Seven devices from a batch of d-HEBs were each etched separately and then measured with a four point probe immediately after being removed from the RIE chamber. For all seven devices, the 1st argon-based RIE was 1.5 minutes long. The average device resistance is 61Ω with a standard deviation of 10Ω. The target resistance for the batch was 70Ω (at room temperature, or 35Ω at 4K). The average L/W ratio for this batch is 1.96, giving an average sheet resistance of 31.1Ω/□.

Variations in the parameters of the reactive ion etch steps probably influence the resistance distribution significantly. For instance, a five second extension of the $SF_6$-based etch of the HEB niobium is actually a 17% over-etch, which is plenty of time for fluorine radicals to continue narrowing the bridge width. A five second variation in etch time is certainly understandable, especially given that the automatic RF tuning network of the RIE often requires the operator to override it, which can cost several seconds.

Time variations can be minimized by increasing the etch time while decreasing the etch power accordingly; a 60 second long etch with a 55mW/cm² RF power density for the HEB niobium etch step would achieve the same results as a 30 second long etch using 110mW/cm² of RF power density, while halving the over-etch error.

A cryogenic measurement of device resistance versus temperature is presented in Figure 12, which shows device resistance as a function of temperature for an HEB device fabricated atop silicon. For these cryogenic DC measurements, the bolometer is mounted
onto the end of a dip-stick and submerged into liquid helium. Slowly moving the end of
the dip-stick in and out of the helium varies the operating temperature of the device.
Devices are measured using a four point probe and a current bias of around 10μA. The
results in Figures 12 show the expected steep transition in resistance as temperature is
increased beyond the transition temperature of the microbridge.

![Graph showing resistance versus temperature measurements](image)

**Figure 12** Resistance versus temperature measurements of a diffusion-cooled hot-electron bolometer microbridge fabricated on silicon.

### 5.3 References

Karasik, A.D. Semenov, “Millimeter and Submillimeter Range Mixer Based on
Electronic Heating of Superconducting Films in the Resistive State,” *Superconductivity*,
3, pp. 1582-1597, 1990


Chapter 6

Fabrication of Phonon-Cooled Hot-Electron Bolometers

The fabrication process for phonon-cooled HEBs is similar in many aspects to that for diffusion-cooled HEBs since the physical structure of the two devices are closely related. Both devices are fabricated from thin films of superconducting materials, with thick metal pads defining the device length. However, the sheet resistance of the thin absorber film of the microbridge differs significantly between the two devices for two reasons. First, we fabricate our p-HEBs from thin films of NbN, which has a higher resistivity than niobium. The resistivity of niobium is \(~350\mu\Omega\text{cm}\) versus \(~4000\mu\Omega\text{cm}\) for our NbN thin films. And second, the NbN film in a p-HEB is much thinner than the niobium film in a d-HEB. For p-HEBs, where phonons must escape from the absorber material to the substrate before interacting with electrons, the film must be extremely thin\,[1]\). For our devices, the NbN is only 4\text{nm} thick. Just above the transition temperature (around 10K), we find that our NbN has a sheet resistance of around \(1k\Omega/\square\), compared with a sheet resistance of only \(35\Omega/\square\) for niobium. Therefore, in order to obtain a reasonable device resistance (35\(\Omega\) to 100\(\Omega\), typically), a p-HEB is usually 3\text{\mu m} to 4\text{\mu m} wide, compared to a d-HEB width of around 100\text{nm}.

The larger bridge width of p-HEBs relaxes the tolerance of that dimension, which in turn eases the fabrication process. In addition, the larger bridge volume greatly reduces the susceptibility of the device to electrostatic discharge compared to the extremely sensitive d-HEBs. For this reason, p-HEBs are less likely to open circuit during handling and are therefore a more robust device than the d-HEBs.
6.1 p-HEB Fabrication

For the sake of discussion, I have divided the discussion of my p-HEB fabrication process into four sections: (i) NbN deposition (ii) HEB bridge length definition (iii) fabrication of the NbN microbridge etch mask, and (iv) etch of the HEB bridge. The process is self-passivating, so a final passivation step is not necessary, as is the case with d-HEBs. Figure 1 outlines the p-HEB fabrication process.
6.1.1 NbN Film Deposition

The NbN films for our work are deposited at Moscow State Pedagogical University in Russia. Deposition takes place in a reactive vacuum environment of argon and nitrogen, with the substrate stage heated to 900°C. Niobium sputtered from a DC magnetron source reacts with the nitrogen, forming NbN atop the heated substrate [2-4]. Researchers at the National Institute of Standards and Technology in Boulder, Colorado use a similar process for depositing NbN [5].

In order to integrate the p-HEBs onto ultra-thin silicon chips, the NbN thin films are deposited atop the device layer of SOI substrates. The critical temperatures (T_c) of the films, as measured at Moscow State, range between 10K and 11K. Figure 1 shows a resistive transition of a NbN film, which was measured using the facilities at the University of Virginia. The film in the Figure has a critical temperature of 9.9K and a transition width, ΔT, of 1.3K. We find that the sheet resistance of our films actually increases as temperature decreases. The resistance ratio, comparing the room temperature resistance (R_{RT}) to the resistance just above the critical temperature (R_c), has consistently been found to be around 1.3 for both our bulk sheet films and our devices.

The critical temperature, T_c, is defined in this dissertation as the temperature at which the bolometer resistance is 10% of the maximum value just above T_c. Likewise, the transition width is calculated by taking the difference between the temperatures where the bolometer resistances are 10% and 90% of the maximum value just above T_c.
Figure 2  The plot of resistance versus temperature for a NbN thin film shows a sudden drop in resistance at the critical temperature, $T_c$. The above plot is derived from a measurement of a 4nm thin film of NbN using a four-point probe contact method. The film has a $T_c = 9.9\text{K}$, and a transition width $\Delta T = 1.3\text{K}$. The ratio of the film resistance at room temperature ($R_{RT}$) and the resistance just above $T_c$ ($R_c$) is $R_c/R_{RT} = 1.37$. Gold contact pads were fabricated atop the sample in order to facilitate contact between the probe tips and the thin film.

6.1.2 Bridge Length Definition

After receiving the substrates from Moscow State, we dice them into smaller wafers, each measuring two centimeters on a side. The micron-scale features of the wafer, such as RF filters and bowtie antennae, are then fabricated atop the NbN using standard optical lithography in a lift-off process. These structures are formed from a 200nm thick film of gold, which is deposited atop the wafer using electron-beam evaporation. Prior to evaporating the gold, a 10nm thick titanium layer is evaporate in order to promote adhesion between the gold and the NbN; our evaporation system does
not have an ion gun, so the wafers cannot be \textit{in-situ} ion cleaned prior to evaporating the gold layer. The patterns are complete following lift-off, as shown in Figure 1.1.

After defining the micron-scale patterns of the circuit, and as is done in the d-HEB fabrication process, a bilayer of PMMA resists is spun atop the wafer. An electron-beam lithography process then aligns and exposes a pair of patterns that define the length of the NbN microbridge. It is important to note in contrast to the d-HEB devices that these patterns are not cooling pads; the p-HEB thermal cooling process takes place between the absorber material and the substrate via phonon diffusion, unlike in the d-HEB case where electrons diffuse out of the absorber region and into the large thermal heat sinks provided by the cooling pads at the ends of the microbridge. Instead, the patterns at the end of the microbridge define the length of the bridge, across which the LO and RF voltages are applied. The bridge length, along with the bridge width and NbN sheet resistance, determines the RF resistance of the bolometer.

Because of the high sheet resistance of NbN, the microbridge of a p-HEB is typically 3\(\mu\)m to 4\(\mu\)m wide, much wider than the cooling pads of d-HEB devices. Figure 3 shows an SEM micrograph of a pair of these patterns. The bridge length in the Figure is 200\(\text{nm}\), while the pattern widths are designed to accommodate bridge widths of around 3.8\(\mu\)m.

A stack of three metal layers combines to form the bridge length pattern. These are, in order of deposition, 10nm of titanium, 50nm of gold, and finally another 10nm of titanium. The first layer of titanium promotes adhesion between the NbN and the 50nm gold layer. The 50nm gold layer forms an extension of the bowtie antenna, and thereby defines the length of the bolometer microbridge (also shown in Figure 1.2). The second
titanium layer provides adhesion between the gold and an SiOₓ pattern, which is added in a later step to define the microbridge width and passivate the absorber material.

Figure 3 The bridge length of a phonon-cooled HEB is defined by electron-beam lithography and lift-off. Typical bridge length is 200nm or less. The patterns must be wide enough to accommodate a device width of 3µm or greater.

6.1.3 Bridge Width Definition

After defining the bridge length patterns, another bilayer of PMMA is spun atop the wafer and exposed using NPGS. The exposed pattern is simply a rectangle, centered atop the bridge length patterns and covering most of the absorber material between them. After writing and developing the rectangular pattern, a 150nm layer of SiOₓ is thermally evaporated atop the wafer. Following lift-off in heated TCE, a rectangular pattern of SiOₓ remains, spanning the microbridge as shown in Figure 1.3. The SiOₓ pattern serves as an etch mask during a reactive ion etch of the open-field NbN. Figure 4 shows an SEM micrograph of an SiOₓ microbridge mask pattern (also shown in Figure 1.4).
Figure 4 A rectangular pattern of SiO$_x$ is defined between the cooling pads using a combination of electron-beam lithography and lift-off. The SiO$_x$ pattern serves both as an etch mask for the NbN and as a passivation layer of the underlying NbN. The devices from batch 40210R have average dimensions of 164nm long, 4.05$\mu$m wide and 4nm thick.

6.1.4 NbN Etching

We etch the NbN absorber layer with an SF$_6$-based reactive ion etch process, developed in-house and based on our niobium etch processes. The etch chemistry consists of SF$_6$ (13.5sccm), CHF$_3$ (10.6sccm), and N$_2$ (1.6sccm). At a pressure of 30mT and with an RF power density of 55mW/cm$^2$, the etch rate is around 6nm/minute. The process requires approximately 50 seconds to fully remove the 4nm of NbN, including a 10 second over-etch period.

The 4nm thin film of NbN atop the silicon substrate is too thin to observe optically, either with the naked eye or through a microscope. As a result, a visual inspection cannot determine when a film has etched away. Instead, the etch processing conditions, including etch time and power, were calibrated using samples of NbN films atop silicon without any other patterns present. These un-patterned wafers allowed the
sheet resistance to be measured prior to and after etching the films. Sheet resistance was measured using a four-point probe station.

The SiO$_x$ masking pattern is not removed from atop the microbridge after the reactive ion etch process. Instead, it remains in place and serves as a passivation layer for the underlying NbN. The presence of the SiO$_x$ atop the absorber material prevents degradation by chemical contamination. Such contamination may occur after fabrication from contaminants in the mixer block or cryostat. For example, a fluorinated polymer or grease within the receiver assembly could come into contact with the microbridge and damage the NbN. Additionally, the SiO$_x$ protects the NbN from chemical etching during subsequent processing steps that define the gold beam leads and the extents of the ultra-thin silicon substrate.

6.2 Results

A cryogenic measurement of device resistance versus temperature is presented in Figure 5, which shows device resistance as a function of temperature for a p-HEB device fabricated atop silicon. As is done with the d-HEB cryogenic measurements, the bolometer is mounted onto the end of a dipstick and submerged into liquid helium. By slowly moving the end of the dipstick in and out of the helium, the operating temperature of the device varies, so the device resistance changes accordingly. Devices are measured using a four-point probe, with a current bias of around 10$\mu$A. The results in Figures 5 show the expected steep transition in resistance as temperature is increased beyond the transition temperature of the microbridge. Notice that in comparison with the curve traced from the bulk sheet film shown in Figure 2, the transition temperature of the NbN
thin film in the device is lower by around 1K while the transition width is around 0.3K wider.

Figure 5 The superconducting transition characteristics of a phonon-cooled HEB are slightly different than that of a thin film of NbN. For one, the critical temperature, $T_c$, is reduced by around a degree. Also, the transition width is wider, typically by around 0.3K. The above device has a $T_c = 9.0\text{K}$ and a $\Delta T = 1.6\text{K}$.

During the early stages of developing the p-HEB fabrication process, we found that the $R_c/R_{RT}$ ratio of the p-HEB devices was much higher than the bulk sheet value of 1.3, and in fact, the ratio was around 2.3 or higher, as is shown in the top two rows of Table 1. This result was unexpected and its cause is still not understood. The higher ratio also presents a problem for device fabrication since a 200nm long bridge would require a bridge width of more than 10$\mu$m in order to achieve a device resistance of 35$\Omega$. Such a long and narrow pad spacing is difficult to achieve using electron-beam lithography as there is simply more area available for debris contamination across the bridge. The larger potential for debris contamination reduces batch yields. The higher
sheet resistance at cryogenic temperatures could alternatively be compensated by shortening the bridge length, which would allow the bridge width to remain relatively narrow. However, using bridge lengths shorter than 200nm also reduces device yield since the lift-off of long and narrow bridges is more difficult, especially, and ironically, when using a bilayer resist structure.

In addition, a large device on the order of 10μm or so can no longer be considered a lumped element for RF circuit analysis. Such a large bridge width is on the order of the bowtie antenna dimensions and so the bolometer dimensions would have to be taken into account when designing the layout of the bowtie antenna. The bowtie antenna is fabricated using conventional photolithography from a set master mask. Once the mask has been fabricated, the bowtie antenna dimensions cannot be varied if, for instance, it is found that the thickness of the NbN film has deviated from expectation. By maintaining small device dimensions, the bolometer may be considered a lumped element having no effect on the functionality of the bowtie antenna.

After further experimentation, I found, however, that the $R_c/R_{RT}$ ratio falls back down to the bulk sheet value when the substrate is subjected to a low temperature anneal. Table 1 relates $T_c$, $\Delta T$ and the $R_c/R_{RT}$ ratio to the annealing time and temperature. Annealing the substrates after completing the electron-beam lithography processes, and just prior to etching the open-field NbN, results in the desired reduction in the $R_c/R_{RT}$ ratio. However, depending on the anneal time and temperature, a decrease in $T_c$ and an increase in $\Delta T$ may also occur due to the anneal process, but the deviations may be minimized while still achieving the reduction in $R_c/R_{RT}$ ratio if the annealing conditions are chosen correctly. We find that a 30 minute anneal at 160C results in a return of the
Rc/R_{RT} ratio to 1.3, while at the same time minimizing a decrease in T_c and a widening of ΔT. Uzawa et al report similar results from their 3nm thick NbN p-HEB devices; they measure an Rc/R_{RT} ratio of 1.35, a ΔT of about 2K wide, and a T_c around 8.5K [6].

<table>
<thead>
<tr>
<th>Device</th>
<th>Anneal (°C)</th>
<th>Anneal (m)</th>
<th>T_c (K)</th>
<th>ΔT (K)</th>
<th>Rc/R_{RT}</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>none</td>
<td>none</td>
<td>9.0</td>
<td>1.3</td>
<td>2.48</td>
</tr>
<tr>
<td>2</td>
<td>none</td>
<td>none</td>
<td>9.2</td>
<td>1.3</td>
<td>2.26</td>
</tr>
<tr>
<td>6</td>
<td>160</td>
<td>30</td>
<td>9.0</td>
<td>1.6</td>
<td>1.31</td>
</tr>
<tr>
<td>7</td>
<td>160</td>
<td>45</td>
<td>8.6</td>
<td>1.5</td>
<td>1.32</td>
</tr>
<tr>
<td>9</td>
<td>180</td>
<td>30</td>
<td>8.2</td>
<td>1.8</td>
<td>1.29</td>
</tr>
<tr>
<td>Uzawa</td>
<td>N/A</td>
<td>N/A</td>
<td>8.5</td>
<td>2</td>
<td>1.35</td>
</tr>
</tbody>
</table>

Table 1 Prior to etching the open field NbN, the wafer is subjected to an anneal, which determines the critical temperature (T_c), the transition width (ΔT), and the ratio of the device resistance at room temperature (R_{RT}) and to that just above T_c (R_c). In order to keep Rc/R_{RT} low, the wafer is annealed on a hot plate. However, if the anneal time is too long or the anneal temperature too high, then T_c may be reduced and ΔT may widen. In addition to reducing Rc/R_{RT}, annealing also reduces the device resistance, which is shown in Figure 2. Devices are from the 40114M4 batch. Results published by Uzawa et al are included in the bottom row for comparison [6].

The reactive ion etch process used to define the bridge width also affects the resistance of the bolometer. Longer etch times and etch powers result in increases in the device resistance. In Table 2, the room temperature sheet resistance, R_{RT}, is presented along with anneal temperature, anneal time, and the Watt-minute product associated with the RIE process. The Watt-minute product is simply the product of the applied RIE RF power and the etch time, and is the amount of energy applied to the substrate during the etch process. By minimizing the amount of time and energy that the substrate is exposed to, R_{RT} is also minimized. However, a certain amount of etch time and energy is required to remove the NbN; for a 4nm thick film of NbN, we find that a minimum of 27Wm is required to completely remove the film.
<table>
<thead>
<tr>
<th>Device</th>
<th>Anneal (°C)</th>
<th>Anneal (m)</th>
<th>RIE (Wm)</th>
<th>$T_c$ (K)</th>
<th>$R_{RT}$ ($\Omega/\square$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>none</td>
<td>none</td>
<td>60</td>
<td>9.0</td>
<td>1384</td>
</tr>
<tr>
<td>2</td>
<td>none</td>
<td>none</td>
<td>40</td>
<td>9.2</td>
<td>1359</td>
</tr>
<tr>
<td>6</td>
<td>160</td>
<td>30</td>
<td>80</td>
<td>9.0</td>
<td>863</td>
</tr>
<tr>
<td>7</td>
<td>160</td>
<td>45</td>
<td>80</td>
<td>8.6</td>
<td>925</td>
</tr>
<tr>
<td>8</td>
<td>160</td>
<td>30</td>
<td>33</td>
<td>8.8</td>
<td>773</td>
</tr>
<tr>
<td>9</td>
<td>180</td>
<td>30</td>
<td>33</td>
<td>8.2</td>
<td>758</td>
</tr>
</tbody>
</table>

Table 2  Sheet resistance of NbN is affected by both annealing and RIE etch conditions. In the above Table, the RIE etch conditions are represented by Watt-minutes, or the product of etch time and etch power. Decreasing the Watt-minutes reduces device resistance. However, this parameter can only be reduced so far; the minimum Watt-minutes required to remove 4nm of NbN is 27Wm. Further reduction in device resistance is achieved by increasing the annealing temperature. However, increasing the annealing temperature reduces $T_c$ and increases $\Delta T$, and if annealed at 200°C or greater the NbN no longer superconducts at all. Devices are from the 40114M4 batch.

A large Watt-minute product implies that the substrate is exposed to excessive chemical attack beyond what is necessary to remove the open-field NbN. We suspect that increased exposure to the highly electronegative ionized fluorine within the RIE etch chemistry damages the NbN under the SiO$_x$ mask along the pattern perimeter. By extending the etch time, the etch chemistry has more time to damage the perimeter NbN, thereby reducing the effective device width and, correspondingly, increasing the device resistance.

The NbN-based p-HEB bolometers offer a significant advantage over the Nb-based d-HEBs in that the p-HEBs are far less susceptible to damage by electrostatic discharge (ESD). ESD is a significant consideration from the viewpoint of device fabrication and receiver assembly. Researchers at JPL use a circuit layout that incorporates a high resistivity single crystal niobium film in series with the bolometer,
which greatly reduces the ESD problem. At room temperature the resistance of the single
crystal niobium film is quite high, protecting the bolometer, while at the operating
temperature of the mixer the single crystalline film has a zero DC resistance. The RF
resistance of these films at THz frequencies is also quite low, making it suitable as a
circuit element for tuning or filtering. Unfortunately, we presently do not have an UHV
deposition system at UVA with the 900C substrate stage required for the deposition of
such films.

The p-HEBs offer several other significant advantages over the d-HEBs from a
fabrication standpoint. First, our p-HEB fabrication process requires fewer processing
steps than our d-HEB process, which significantly decreases production time. And
second, the device dimensions are far more critical for d-HEBs than they are for p-HEBs,
which simplifies the treatment of the EBL processes.

Despite the advantages noted above, from an RF design engineering point of view
the p-HEBs are sometimes less preferable than their d-HEB counterparts because the p-
HEBs do not offer the wider IF bandwidth that the d-HEBs provide. A wide IF
bandwidth is desirable in THz heterodyne mixers since there is currently a dearth of
tunable local oscillator sources available in the THz regime. By using devices with wide
IF bandwidths, the RF engineer can cover more of the THz spectrum with a single local
oscillator source, which is often an un-tunable CO2-pumped far-infrared laser [7]. The
emission lines of such sources are often several gigahertz away from the spectral lines of
interest to scientists and astronomers, so a wide IF bandwidth is important if one wishes
to cover multiple spectral lines with a single receiver. The difference in IF bandwidth
between the two devices is attributed to the faster thermal response time of the diffusion
cooling mechanism in the d-HEB devices. NbN-based p-HEBs typically have an IF bandwidth of around 1GHz to 4GHz, while diffusion-cooled HEBs may have IF bandwidths approaching 10GHz [8-10].

6.3 References


Chapter 7

Results and Conclusions

In order to determine the feasibility of using ultra-thin silicon chips in the microstrip channel of a THz receiver, we mounted several of these chips within our 585GHz mixer blocks, then cooled the blocks to 4.2K in a cryostat. All of the chips featured NbN p-HEBs as the non-linear mixing element, which allowed for current-voltage (I-V) and resistance-temperature (R-T) curves to be measured. These measurements established the presence of electrical continuity through the chips, as well as the non-linear response of the p-HEBs with respect to temperature and current, implying that the chips remain whole and in electrical contact with the block after assembly and cool-down. In this chapter, we discuss the receiver assembly process, describe the cryogenic testing, and then compare the cryogenic I-V characteristic from the bolometers within the receiver blocks to I-V characteristics from DC devices that were dip-stick tested in a liquid helium dewar.

7.1 Cryogenic Device Testing

Prior to measuring our bolometers on ultra-thin silicon chips in the cryostat, we measured the I-V and R-T relationships of p-HEB devices fabricated on thick (350μm) silicon substrates. These devices are designed specifically for DC cryogenic testing, featuring large gold contact pads for four-point probe measurements. One bolometer fits within a cavity at the end of a dipstick, which is then submerged within liquid helium in order to bring the temperature of the bolometer down below the critical temperature. In addition to the four-point probe, the dipstick also features a small resistive heater and a
thermometer that allow the operating temperature of the bolometers to be accurately controlled with a PID feedback system.

Several characteristic device parameters derive from the data obtained from DC cryogenic testing. One of these is the critical current density of the NbN thin film. High quality NbN thin films have a critical current density, $j_c$, as high as $2 \times 10^7 \text{A/cm}^2$ [1]. However, bolometers made from NbN thin films tend to show a critical current density that is generally an order of magnitude lower than that of high quality bulk films. For instance, researchers from the Harvard-Smithsonian Center for Astrophysics and the California Institute of Technology report of a $2\mu\text{m}$ wide, $4\text{nm}$ thick NbN p-HEB that has a critical current of $85\mu\text{A}$, which gives a critical current density of $1.1 \times 10^6 \text{A/cm}^2$ [2,3]. The NbN films used in their work were grown by the same group at Moscow State Pedagogical University who grew the thin films used in this dissertation. A cooperation of researchers from Chalmers University of Technology in Gothenburg, Sweden and the Kansai Advanced Research Center in Kobe, Japan measured a critical current density of $0.7 \times 10^6 \text{A/cm}^2$ for a $3\text{nm}$ thick NbN device at 4.2K [4]. Their films were also grown by the Moscow State group. A third group, from the National Institute of Standards & Technology (NIST) and the University of Massachusetts Department of Astronomy, give data and figures that indicate a critical current density of around $1.1 \times 10^6 \text{A/cm}^2$ at 4K [5]. The NbN thin films used in their work were grown by the group at NIST.

Measuring the critical current of a bolometer and comparing the result to previously recorded values indicates whether the NbN film is localized within the intended microbridge area or if there is still unetched NbN outside the bridge area. Alternatively, and due to the high resistivity of NbN, a R-T curve could still be plotted if
the open-field NbN was not removed. By measuring the critical current density, the absence of the open-field NbN is proven if the critical current density compares in magnitude to an expected value.

**Figure 1** Current-voltage (I-V) characteristics of a NbN bolometer were traced by sourcing DC current through the bolometer while the substrate was maintained at specific operating temperatures. At temperatures of 10K and above, the I-V relationship is nearly linear. However, as the device is cooled into the transition region, the I-V relationship becomes highly nonlinear. The nonlinearity results because of a self-heating affect within the bolometer; at low currents, the resistance is small as dictated by the R-T curve (Figure 2). As the current increases, the bolometer heats up locally even though the bath temperature remains constant. This results in an increase in resistance, which approaches the normal-state resistance asymptotically as the source current is ramped further. When the bolometer is current-sourced while the substrate is below the critical temperature, the device superconducts until the critical current density ($j_c$) is exceeded (a small resistance is measured below the critical current due to contact resistance between the device and the measurement probes). Once beyond $j_c$, the voltage jumps to $V = j_cAR(T)$. If the current is then decreased below the critical current, the bolometer does not revert to the superconducting state immediately due to the self-heating affect. Only after the self-heating affect is too small to sustain the bridge temperature above $T_c$ will the bolometer again superconduct. The temperatures of the I-V plots shown in this Figure are indicated in the R-T curve of Figure 2 by vertical, color-coded lines.

The I-V curves presented in Figure 1 are from one of our NbN bolometers, which measures 2.34μm wide by 210nm long by 4nm thick. Using our dipstick system, we measured a critical current of 237μA at 6.2K, which gives a critical current density of 2.5x10⁶A/cm²; a value comparable to the figures presented by other researchers. As shown in the R-T curve of Figure 2, this device has a $T_c$ of 8.2K, a $\Delta T$ width of 1.8K and resistance of 87Ω at 13K. The $R_c/R_{RT}$ ratio is 1.29.
The resistance versus temperature (R-T) relationship of the device measured for the Figure 1 I-V data is shown above. The device has a $T_c$ of 8.2K, a $\Delta T$ width of 1.8K, and resistance of $87\Omega$ at 13K ($R_c$). The device is 2.34$\mu$m wide, 210nm long and 4nm thick. The curve was traced using a source current of 10$\mu$A, which is low enough to prevent self-heating from dominating the curve characteristics. The color-coded vertical lines indicate the operating temperatures at which the I-V data of Figure 1 were measured. The critical temperature, $T_c$, is defined in this dissertation as the temperature at which the bolometer resistance is 10% of the maximum value just above $T_c$. Likewise, the transition width is calculated by taking the difference between the temperatures where the bolometer resistances are 10% and 90% of the maximum value just above $T_c$.

We plotted the I-V characteristics by sourcing the bolometer with a DC current while maintaining the substrate at specific operating temperatures. At 10K, the device behaves like a traditional resistor, and shows a nearly linear relationship between current and voltage. However, as the operating temperature is decreased, the resistance of the device decreases as dictated by the R-T relationship (Figure 2). For measurements made while maintaining the substrate temperature within the transition region, the resistance remains low for small currents, but increases non-linearly as the current increases. This rise in resistance results from a self-heating affect within the bolometer; the source current locally heats the NbN bridge, resulting in an increase in resistance. At higher
currents, the resistance tends asymptotically towards the normal state value. This nonlinear I-V relationship is shown in Figure 1 for operating temperatures of 8.2K, 7.9K and 7.6K, which are all located along the toe of the R-T curve (see Figure 2) at or below T_c. If the operating temperature is less than the critical temperature, then the device superconducts so long as the current density remains below the critical current density. The 6.2K measurement presented in Figure 1 does show a small resistance below the critical current due to contact resistance between the NbN and the gold contact pads. Once the current is sourced beyond the critical current density, the bolometer reverts back to the normal conducting state and the voltage across the bolometer jumps to the corresponding normal state value, V = j_cAR(T). If the current is then decreased below the critical current value, the device does not immediately begin to superconduct again due to the self-heating affect; only after the self-heating affect is too low to sustain the bolometer temperature above the critical temperature will the device begin to superconduct again. This discontinuous I-V relationship is demonstrated in the 6.2K measurement of Figure 1. Arrows in the Figure indicate discontinuities along the I-V path.

7.2 Receiver Assembly, DC Testing and Results

Two mixer blocks were machined by Custom Microwave Inc., a company specializing in the machining of precision microwave components. The blocks are brass and are finished with a 5μm thick layer of plated gold. Figure 3 shows a photograph of the lower block half mating face. Inset within the Figure is a close up of the microstrip channel (vertical structure, inset) and backshort (left, inset). After receiving the two finished mixer blocks from Custom Microwaves, we inspected the dimensions of the
microstrip channels, backshorts, and reduced-height waveguides with an optical microscope, and compared the measurements to the AutoCAD drawings presented in Chapter 5. In general, the dimensions of the machined block dimensions compare favorably with CAD specifications, though it should be noted that the measurements made with the optical microscope are only accurate to within a few microns.

Figure 3 The receiver blocks were machined by Custom Microwaves, Inc. The above image shows the junction between the reduced-height waveguide and the microstrip channel. On the top right, the reduced-height waveguide intersects with the feedhorn antenna. In the inset, A close-up picture of the receiver shows the microstrip channel (vertical structure) and the backshort (left).

The microstrip channels for all four block halves are uniformly around 80μm wide, which is extremely important given that the mixer chips are only 76μm wide and must fit within the microstrip channels. The microstrip channel depths are also measurably close to specification, within the +/-5μm tolerance specified by Custom Microwave. Due to the limitations of the milling machine tools, both the backshort and the RF end of the microstrip channels are rounded, with a radius of curvature of around 40μm. The rounding is not a problem for the microstrip channel since it is situated at the far end of the RF filter structure. As for the backshort, it is uncertain if the rounding will
have a significant impact on receiver performance; HFSS simulations of backshort length variation show that deviations by +/-15μm have a minimal impact on RF performance.

7.2.1 Receiver Assembly

Shown in Figure 4 is an ultra-thin silicon chip with gold beam leads and integrated RF circuitry fitted into the microstrip channel of a receiver block. The chip is gently nudged into place using a three-axis micromanipulator featuring a fine-point probe. The IF beam lead (left side of the Figure) attaches to an IF microstrip line, which leads to a 50Ω SMA port, via conductive epoxy (epoxy not shown in the Figure).

Figure 4 An ultra-thin silicon chip rests within the microstrip channel of the 585GHz test receiver. The chip is suspended in the middle of the microstrip channel by the beam leads that extend from the chip perimeter. The leftmost beam lead contacts the IF port, which is a gold microstrip line atop a quartz substrate that leads to an external IF low-noise amplifier.

The IF microstrip line is a 50Ω strip of gold fabricated atop a 250μm thick quartz substrate that fits within the recessed block cavity adjacent to the microstrip channel. The quartz chip is manually lapped with 600 grit sandpaper to around 250μm thick, or until the top of the chip is just a few microns below the mating face of the block. The
extra spacing provides some room for the conductive epoxy. Clear fingernail polish secures the quartz chip to the IF cavity. The fingernail polish is robust enough to hold the chip in place through thermal cycling and provides decent thermal conductivity between the mixer block and the chip [6]. Opposite the mixer end of the IF microstrip line is the 50Ω SMA connector, which is secured to the outside of the mixer block. The inner conductor of the SMA connector is soldered directly to the IF microstrip line. Joining the two block halves together compresses the RF beam lead (far right in Figure 4) and the smaller structural beam leads along the length of the chip, thereby securing the chip near the middle of the microstrip channel. Three pins, which fit into holes machined into both halves of the mixer block, precisely align the block halves. The halves are held together with a set of four 2-56 thru-tapped screws.

### 7.2.2 DC Testing

The initial test performed after assembling a receiver consists simply of measuring the resistance of the block between the inner and outer conductors of the SMA port. If the chip fits securely within the microstrip channel, and the beam leads survived being compressed between the two block halves, then a resistance is measured, indicating electrical continuity from the IF port, through the RF circuitry and the HEB mixing element, to the RF ground port.

Next, the assembled receiver block is cooled to 77K by submerging it in liquid nitrogen in order to test the durability of the ultra-thin silicon chip, the quartz IF chip, and the gold beam leads through thermal cycling. If an open circuit develops during their initial cool-down, then the circuit has lost electrical continuity with the external measurement equipment due to thermal contractions as the temperature decreased. A
discontinuity most likely would develop in locations where three or more materials interact, such as between the quartz IF chip and the SMA center conductor, or between the quartz IF chip and the IF beam lead. Determining whether or not a block will open during cool-down prior to loading the block into the cryostat can save a considerable amount of time; if the block is found to become open when cooling inside the cryostat, the entire cryostat must be brought back up to room temperature, which often takes more than twenty-four hours. Once the thermal cycling durability is established, the block is considered ready for cooling down to 4.2K.

In order to cool the mixer block down to below $T_c$, we mount the block atop the cold platter of a cryostat. For DC I-V measurements, the block does not attach directly to the cold platter. Instead, it is secured against a copper brace, which is then bolted to the cold platter. A 0.5mm thick sheet of Teflon placed between the cold platter and the copper block slows the flow of heat between the block and the cold plate during thermal cycling. In addition to the block, the copper brace also has a heater (a 60Ω resistor) connected to it, and a diode thermometer is attached to the mixer block. With the Teflon spacer, heater and thermometer, we are able to control the temperature of the mixer block to within less than a tenth of a Kelvin. Once held at constant temperature, I-V characteristics of the mixing element within the receiver block may be reliably measured.

Heat flow through a solid of uniform cross-section is dictated by Equation 1,

$$Q = \frac{A}{d} \int_{T_1}^{T_2} KdT$$  \hspace{1cm} \text{Equation 1}$$

where $A$ is the cross-sectional area, $d$ is the thickness of the space between the two heat reservoirs, while $T_1$ and $T_2$ are the temperatures of the adjacent reservoirs. $K$ is the thermal conductivity of the spacer material, and is dependant on the difference between
$T_1$ and $T_2$ ($\Delta T$). However, material-dependant curves of $K$ as a function of $T$ may be used to determine the integral $KdT$, thereby simplifying the analysis. For a Teflon spacer and a $\Delta T$ of 10K, the value of the $KdT$ integral is around 4.4mW/cm. With a 4.72cm$^2$ copper footprint and a Teflon thickness of 0.5mm, we estimate a heat flow of 400mW between the copper brace and the cold plate for a $\Delta T = 10K$. For a $\Delta T = 300K$, the $KdT$ integral is around 700mW/cm, giving a heat flow of 65W. The maximum power output from the resistive heater is limited to 500mW, so the 0.5mm Teflon spacer is sufficient for limiting heat flow at low values of $\Delta T$ while maintaining a large heat flow for higher values of $\Delta T$ so that the mixer block may cool down to below $T_c$ within a reasonable timeframe.

![Figure 5](image)

**Figure 5** Current-Voltage curves from a device mounted within the 585GHz HEB receiver block resemble the curves presented in Figure 1. The batch from which this device was drawn has average dimensions of 164nm long, 4.05µm wide and 4nm thick. The critical current at 4.8K is $10^5$A, giving a critical current density of $0.66x10^6$A/cm$^2$. These curves demonstrate our ability to fabricate hot-electron bolometers on ultra-thin silicon chips with beam leads, mount those chips within the microstrip channel of a mixer block, and cool the entire assembly down to cryogenic temperatures. A 3Ω series resistance is introduced through the measurement connections and the IF filter structures on the ultra-thin silicon chip, as indicated by the steep I-V response observed while the bolometer is superconducting.

Current-voltage curves from cryogenic testing of a NbN device mounted within a mixer block are shown in Figure 5. As was done for the I-V measurements with our DC
dipstick-mounted bolometers, we measured I-V curves at several temperatures around the transition region of the R-T curve. The I-V curves presented in Figure 5 show the same characteristics as those presented in Figure 1, with the self-heating affect causing a non-linear response for temperatures around $T_c$. In particular, the curves plotted at 4.8K, 6K and 7K all show that the device superconducts until the current within the device exceeds the critical current density. These three curves also demonstrate the self-heating affect, indicating that, down to a point, current flow less than the value of the critical current dissipates enough heat within the microbridge to maintain a local temperature above the critical temperature. These I-V measurements demonstrate our ability to fabricate hot-electron bolometers on ultra-thin silicon chips with beam leads, mount those chips within the microstrip channel of a metal waveguide block, and cool the entire assembly down to liquid helium temperatures.

7.2.3 Disassembly

The 585GHz HEB receiver is disassembled by separating the two block halves and extracted the ultra-thin silicon chip from the microstrip channel. After separating the two block halves, the chip tends to adhere to the mating face of the top block half, as shown in Figure 6. This preferential adhesion results because the plated gold on the top of the beam leads has a greater surface area than the evaporated gold on the bottom of the beam leads. In addition, plated gold tends to be softer than evaporated gold, and so conforms to a mating face to a greater degree than evaporated gold when placed under stress.

The gold beam leads do not adhere permanently to the face of the block. Instead, we find that the beam leads remain attached to the silicon chip as it is peeled away from
the block mating face using the micromanipulator probe tip. To remove the chip, the probe tip is slowly moved through the microstrip channel under the chip, starting at the IF cavity and working towards the RF end of the channel. This motion causes the chip to lift up and the beam leads to peel away from the mating face. The IF beam lead peels away easily from the conductive epoxy while separating the block halves. After removing the chip from the microstrip channel, and gently scraping away the conductive epoxy from the IF quartz chip, the receiver is ready for re-assembling.

![Figure 6](image)

**Figure 6** After separating the two halves of the mixer, the chip sticks to the mating face of the top block half, becoming disconnected from the conductive epoxy attachment at the IF beam lead. Because the chip adheres to the top block half, the RF circuitry is not visible.

Because the mating faces are plated with gold, the beam leads create indentations along the microstrip channel where the beam leads were crimped between the two block halves. These indentations are less than 0.5\(\mu\)m deep, on order with the lapping scratches present on the mating faces. Figure 7 shows a close-up photograph of several of these indentations, focused on the RF-end of the mixer block mating face.
After disassembling the receiver block halves and removing the chip from the microstrip channel, slight indentations where the beam leads had been remain in both block halves. The beam leads peel away quite easily from the block halves, and remain adhered to the silicon chip.

### 7.3 Future Work

Several research groups associated with THz radio astronomy are interested in pursuing aspects of the technologies presented in this dissertation. Researchers at the National Radio Astronomy Observatory in Charlottesville are currently designing an SIS receiver that will be implemented on both ultra-thin silicon chips (3\(\mu\)m) and quartz chips (50\(\mu\)m) with beam leads. Typical SIS mixers are implemented within waveguides, or in a quasi-optical configuration. Fixed tuned waveguide SIS mixers are commonly used in millimeter wave receivers because, compared to the quasi-optical systems, waveguide feedhorns have cleaner beam patterns, higher beam efficiencies, and are easier to couple to telescopes with low spillover. However, it is much more difficult to develop a submillimeter-wave waveguide SIS receiver because the submillimeter-wave mixer circuits are extremely small and usually fabricated on very thin, fragile substrates such as silicon, gallium arsenide, or quartz. Also, as the frequency of circuits increases, the size
of the circuit housing decreases, the tolerance required for the circuit housing increases and the placement of the circuit become very difficult and critical, making assembly of these devices even more problematic [7].

The ultra-thin silicon beam lead technology developed in this work is particularly well suited for submillimeter-wave waveguide mixers. To demonstrate the advantages of the beam lead technology, a 385GHz to 500GHz SIS mixer with an 8GHz intermediate frequency is currently being developed by NRAO in collaboration with UVa. This mixer will cover the entire 0.6mm to 0.78mm band, which is one of the main atmospheric windows available for conducting ground-based submillimeter-wave observations. An added incentive for developing this mixer is that the Atacama Large Millimeter Array (ALMA) project, currently being funded by an international partnership between the United States (through the NSF), Canada and Europe, has designated this band as its receiver band 8. Since ALMA has decided to implement band 8 in the second phase of its construction, the proposed mixer design, if successful, could also be used as the prototype design for the ALMA band 8 receivers [7].

The advantage of including beam leads on THz chips may be fully realized when assembling large arrays of mixers into a single receiver. This is especially true when the non-linear mixing element of the circuit is a hot-electron bolometer. For HEBs, especially diffusion-cooled HEBs, the fabrication yields are lower than the more mature SIS technology, so it is advantageous to not implement the entire array of devices on a single chip. Instead, each mixing element of the array could be fabricated on its own chip, allowing single devices to be removed from the array and replaced by another element if one is found to be faulty. Such a scheme would allow for the assembly of
large element arrays by removing dependence on the yield statistics of the device fabrication process.

Researchers at the California Institute of Technology and the Steward Observatory at the University of Arizona are interested in assembling large arrays of HEB devices for radio astronomy receivers [8]. Figure 8 shows an HFSS model of a conceptual sixteen-element HEB array. Each element in the array features a single HEB device, which is fabricated atop an ultra-thin silicon chip. The chips are held in place atop a micromachined silicon array frame [9]. The RF and LO signals are directed towards HEB mixing elements via integrated antennae structures and waveguides oriented perpendicular to the plane of the array (not shown in the Figure). The RF ground and LO outputs of each element are contacted to external circuitry on the array frame through gold beam leads. The beam leads also provide thermal contact and mechanical rigidity between the elements and the array frame. Each element within the array is independent of the others from the standpoint of receiver assembly, so single elements from the array may be added or replaced without disturbing the other elements.
Figure 8  Shown is a conceptual model of a sixteen element HEB array, as laid out in HFSS. Each element of the array is housed on its own chip, which may be added or removed without disturbing the other elements of the array. Electrical, mechanical and thermal contact between each element of the array (pink) and the array frame (blue) are made via beam leads.

Limitations on the use of ultra-thin silicon chips in THz receivers will be determined by finding a balance between the requirements of the applications and the physical restrictions of ultra-thin silicon chips. This dissertation shows that it is possible to fabricate silicon chips as thin as 1.6\mu m. In fact, the largest silicon chips with beam leads that were fabricated for this work, measuring 500\mu m by 2000\mu m, were also the thinnest. The chips show no signs of curling due to internal stress from the silicon or from external stress introduced by the gold beam leads and other structures fabricated atop the silicon. In addition, the chips can be reliably handled with a pair of fine tweezers without breaking, and batch yields are excellent.

At what thickness is silicon too thin to handle and therefore no longer applicable for THz receivers? This question may not need to be addressed immediately, at least not from an RF design standpoint, because the assembly of THz receivers is hindered by several other physical limits. Our current results should satisfy RF chip design interests well into the mid-THz regime. As an example, given that it is possible to fabricate
silicon chips as thin as 1.6μm, we could directly scale all of the dimensions of our 585GHz receiver design by a factor of 1.8 (3μm/1.6μm), with the demonstrated 3μm silicon chip circuit, to operate at 1.1THz using 1.6μm thick silicon chips. Additionally, from our HFSS measurements presented in Chapter 5, 10μm silicon chips show similar promise for operating in the 585GHz receiver. Scaling the 10μm design by a factor of 6.25 (10μm/1.6μm) yields a 3.7THz operating frequency for 1.6μm thick chips. However, it should be noted that scaling receiver designs to higher THz frequencies is extremely challenging, not so much because the chips must be thinner, but because the machining of the microstrip channel, backshort, and integrated circuitry becomes increasingly difficult. Directly scaling the 585GHz receiver to 3.7THz, for example, would require a microstrip channel width of only 12.8μm, which is beyond the limits of traditional machining capabilities. In addition, the high-impedance segments of the IF filters would need to be a fairly accurate 1.3μm wide, which is a challenge for conventional contact photolithography. Alternative mixer designs could, of course, also be explored, but it is certainly clear that the limitations on waveguide machining and circuit fabrication will have to be overcome long before the need for thinner silicon chips becomes a restricting design factor. This exercise in scaling simply demonstrates that the ultra-thin silicon chip technology as it currently stands should be able to meet the demands of future THz receiver designs.

Future submillimeter-wave mixer circuits should incorporate more complicated design architectures in order to take full advantage of the beam lead schema. The current method of placing a beam lead chip atop the mating face of a microstrip channel is not a simple process, and it requires a considerable amount of time to orient the chip properly
atop the channel. Larger beam leads, and perhaps even a silicon frame, could be incorporated into the design to facilitate the assembly of receivers. Such designs could integrate with micromachined silicon parts to allow for true drop-in assembling. For example, anisotropic etching of silicon parts along specific crystal planes could be used to build a micromachined frame that would direct the beam lead chip to a specific, aligned position. The chip would naturally come to rest within the recess with the beam leads oriented above the contact points on the micromachined frame, and without having to gently nudge the chip into its proper orientation with a micromanipulator.

7.4 Conclusion

During the course of this work we developed two novel chip and beam lead technologies that have important applications for submillimeter-wavelength detectors as well as possible applications in other fields. The first of these, discussed in detail in Appendix 1, is the first reported beam lead process for quartz-based detectors [10-12]. Our process is a unique planarization process that uses a wafer dicing tool to circumvent the lack of anisotropic, deep quartz etching technologies. The accuracy of chip definition is therefore defined by the dicing error, which is typically +/-5um. This planarization process is actually independent of quartz and so can be applied to almost any other substrate material. The ability to planarize deep-wafer topographies is also a versatile micromachining tool with a wide range of potential applications.

The second technology developed in this dissertation, also a first to be reported, is our ultra-thin silicon chip fabrication process, integrate with gold beam leads for submillimeter-wavelength detectors. Silicon as a substrate material offers several advantages over quartz. The rupture modulus of silicon is much larger than that of quartz
(130MPa versus 50MPa), so micron-scale chips are not too brittle to handle. Also, the thermal conductivity of silicon is much higher (150W/mK versus 2W/mK), which accommodates for the difference in dielectric loss tangent (0.0001 for quartz versus 0.004 for silicon at 10GHz). Dielectric loss tangent is a measure of how much the substrate heats up due to RF radiation propagating within the substrate. One disadvantage of silicon with respect to quartz is the higher dielectric constant (11.9 versus 3.78 at 10GHz). The difference in dielectric constant makes the electrical thickness of a silicon substrate a factor of \((11.9/3.78)^{1/2} = 1.77\) thicker than that of quartz for a given equivalent physical thickness. As an example, a 3µm thick substrate of silicon is equivalent to 5.3µm of quartz or 10.3µm of vacuum. However, a 5.3µm thick quartz substrate cannot be realized due to the brittle nature of quartz whereas a 3µm thick silicon chip can certainly withstand the rigors of receiver assembly and cryogenic cycling.

We developed a process for fabricating ultra-thin silicon chips based on SOI substrates that has yielded robust detector chips as thin as 1.6µm. This process also permits the definition of non-rectangular chip geometries with control of final chip dimensions to +/-2µm. In Figures 9 and 10, high-angled micrographs of an ultra-thin silicon chip show the thin profile of both the silicon chip and gold beam leads. The chip shown in Figures 9 and 10 features RF circuitry, including filter choke segments and a bowtie antenna. We have demonstrated ultra-thin silicon chips as long as 2mm (1.6µm thick) and gold beam leads as long as 250µm (1µm thick).
Figure 9 An SEM micrograph taken at a steep angle shows the profile of an ultra-thin silicon chip. The chip features gold beam leads and RF circuitry, including filter choke structures and a bowtie antenna. The chip is 3μm thick while the beam leads are 2μm thick.

Figure 10 A close-up of Figure 9 shows the gold beam leads and ultra-thin silicon chip. The ultra-thin silicon chip is 3μm thick while the gold beam leads are 2μm thick.

Both of the new technologies are particularly well suited for application in submillimeter-wavelength mixers. The beam leads facilitate the mounting of the chips, ease the machining requirements of the waveguide blocks, and simplify the assembly and
testing requirements of mixer arrays. In order to test the ultra-thin silicon beam lead chips, we also designed and modeled a 585GHz waveguide-based heterodyne receiver, which was adapted from the Harvard-Smithsonian Submillimeter Array receiver designs [13]. The receiver also works well when using 30μm-thick quartz chips with beam leads, so in the future a heterodyne receiver fabricated atop a quartz substrate may also be tested with these blocks. Two blocks have been machined, and the ultra-thin silicon beam lead technology has been demonstrated through DC cryogenic testing.

In this work, admittedly, the IF beam lead in our 585GHz receiver design is contacted to the quartz IF microstrip circuit using a rather traditional method, conductive epoxy. As a result, the assembly process does not take full advantage of the beam lead potential; quick assembly and disassembly of submillimeter-wave circuits suitable for rapid prototyping, quick chip replacement, and construction of large-format arrays. However, the RF beam lead and the smaller mechanical beam leads along the chip length demonstrate the ability of beam leads to suspend a chip within the middle of a microstrip channel while providing electrical, mechanical and thermal continuity between the chip and the receiver block, even after thermal cycling from room temperature to cryogenic temperatures and back again.

Importantly, the beam leads allow ultra-thin silicon chips to be incorporated into the design of terahertz receivers. There exist no circuit contacting methods capable of providing robust electrical continuity to an ultra-thin silicon chip that would not damage the chip or secure it permanently to the receiver housing except beam leads. By using beam leads to secure ultra-thin silicon chips within a microstrip channel, the complexity of the microstrip channel is reduced from an RF design standpoint because most of the
microstrip channel volume may be assumed to be vacuum. Current terahertz mixer
designs must consider the effects of a thick dielectric substrate inside the microstrip
channel when analyzing the propagation and mixing of signals within the receiver. When
using ultra-thin silicon chips to position the submillimeter-wave circuitry within the
microstrip channel, only 3 μm or less of silicon need be considered instead of tens of
microns or more of quartz. The machining of waveguide components is also greatly
simplified when using ultra-thin silicon chips since complex structures need not be
machined within the waveguide channel in order to support thick quartz chips,
conductive wire gaskets, or other non-ideal structures that would require the microstrip
channel shape to deviate from rectangular.

During the last decade, the development of submillimeter-wave astronomy has
dramatically improved our understanding of many important astronomical topics,
including galactic molecular clouds, astrochemistry, star formation and stellar evolution,
the solar system, as well as extragalactic cosmology. Most of these works derive from
submillimeter-wave observations using telescopes equipped with Superconductor-
Insulator-Superconductor (SIS) heterodyne receivers. These receivers are capable of
offering quantum-limited sensitivity and essentially unlimited spectral resolution, but
only over a very narrow bandwidth (~1 to 2 GHz). Future astronomical observatories
will require wide instantaneous frequency coverage that exceeds the capabilities of the
current generation of SIS receivers. The lack of tunable local oscillator (LO) sources in
the submillimeter-wave domain favors the development of heterodyne receivers with
wide instantaneous bandwidths. Therefore, it is very desirable to develop a new
generation of submillimeter-wave receivers with wide instantaneous bandwidths [7].
Also, many interesting spectroscopic lines indicative of unique astronomical phenomena exist above 700GHz, the superconducting gap frequency of niobium. Future radio astronomy observatories will therefore require heterodyne receivers capable of mixing beyond this limit.

Above the gap frequency, niobium reverts to the normal-conducting state causing the matching circuitry of niobium-based SIS receivers to become lossy. Hot-electron bolometers, both diffusion-cooled and phonon-cooled, are capable of meeting the demands of future radio astronomy observatories for a plethora of reasons. Although the noise of hot-electron bolometers does not approach the quantum noise limit like SIS receivers, HEBs do offer low noise and wide instantaneous bandwidth, in addition to operating frequencies beyond the gap frequency of niobium. Superconducting HEBs are extremely sensitive, having a noise equivalent power on the order of $10^{-13}$W/Hz$^{1/2}$, and unlike SIS-based receivers, the maximum operating frequencies of HEBs are not limited by the device material. HEBs are also purely resistive and that resistance is frequency independent, so HEBs do not require the complicated tuning structures that must accommodate submillimeter-wave SIS mixer circuits. Due to the relatively slow thermal response of the cooling mechanisms in HEBs, higher-order harmonics are not produced during the mixing process, so additional filter structures are not required to attenuate these signals. Also, the required LO power for HEBs is very low, in the nano-Watt range, and frequency independent, which reduces the power constraints for LO sources.

During the course of this dissertation research, we developed an electron-beam lithography-based fabrication process for both diffusion-cooled and phonon-cooled hot-electron bolometers. Although HEB fabrication has been realized at other institutions,
establishing a fabrication process here at UVa is important for facilitating other research groups at the University. Already development is underway for fabricating arrays of hot-electron bolometers for quasi-optical receivers, and designs have begun for implementing removable-element HEB array structures such as that presented in Figure 8. The HEB fabrication processes are unique in a couple of aspects. For one, the d-HEB process utilizes a bilayer niobium-gold bridge masking structure that is removed while etching the HEB microbridge, and therefore does not require a subsequent mask-removal processing step. Likewise, the p-HEB fabrication process has a unique masking scheme in that the process is self-passivating; the SiO$_x$ mask remains atop the bridge after etching the open-field NbN, thereby providing protection against contamination.

We recently submitted a proposal to build an ultra-high vacuum sputtering system with a heated stage for the deposition of NbN thin films. This new system will allow us to investigate and optimize material parameters for phonon-cooled hot-electron bolometers. The proposed system has two wafer stages, one that can be raised above 900°C for NbN growth and another that is water-cooled. Both of the stages will have DC and RF biasing capabilities to provide additional methods for influencing the morphology of the NbN thin films [14]. With our own supply of NbN thin films, we will be able to develop a firm understanding of how film quality is affected by processing conditions, and allow us to perfect our fabrication processes, such as reactive ion etching and post-process thermal annealing. Importantly, the independence and flexibility gained from having the ability to grow our own NbN thin films will contribute significantly towards meeting the growing demands of future submillimeter-wave astronomical observatories,
enabling UVa to continue its position of international leadership in both THz technology and astronomical detectors.

In conclusion, we have developed two new powerful fabrication technologies for THz mixer chips. We have also developed an electron-beam lithography-based process at UVa for the fabrication of both diffusion-cooled and phonon-cooled HEBs. Finally, we designed a 585GHz waveguide heterodyne receiver that incorporates ultra-thin silicon beam lead chips, fabricated the HEB mixer circuits on those chips, and demonstrated these new technologies by DC testing the entire receiver assembly at cryogenic temperatures. While a number of astronomical applications have been discussed, practical applications for submillimeter-wave heterodyne receivers are not limited to just radio astronomy. We anticipate long-term growth prospects in a wide range of other research fields, including bio-particle detection, atmospheric spectroscopy, and medical imaging among them, all of which will benefit from the work presented in this dissertation.

7.5 References


Appendix 1

Fabrication of Quartz Chips with Gold Beam Leads

The assembly of superconducting millimeter and submillimeter-wave circuits on quartz substrates becomes increasingly difficult as chip dimensions and design tolerances shrink with increased operating frequency. Currently, RF and ground connections are made by soldering, wire bonding, conductive adhesive, or with conductive wire gaskets. Conductive adhesive, wire bonding, and soldering all attach leads permanently to the circuit. Conductive gaskets have been applied successfully in packaging 200 to 300GHz SIS mixers for many years at NRAO (The National Radio Astronomy Observatory) [1,2]. However, due to the difficulties in machining substrate channels with the precision required at higher frequencies, it is not practical to use conductive gaskets for submillimeter-wave circuits.

None of these techniques is ideal for prototyping tasks where frequently changing circuits are needed. The assembly issues, and also the throughput requirements of large radio astronomy projects such as ALMA (Atacama Large Millimeter Array), suggest the need for a beam lead technology. To facilitate the assembly and throughput of superconducting millimeter and submillimeter-wave circuits, we developed a process for fabricating beam leads atop quartz substrates.

Beam lead processes are well established for silicon and GaAs wafers [3-5]. Most of these processes use selective wet etches that take advantage of anisotropic etching of the substrate due to crystal plane orientation. In these cases, gold beam lead patterns are formed during or after completion of the circuitry fabrication process. Since beam lead
thickness on the order of 2µm are needed for physical robustness, these features are typically plated onto the surface of the wafer. The beam lead feature is then revealed to overhang the substrate with a selective backside wet etch. At present, no similar process exists for quartz wafers; thick quartz layers cannot be etched anisotropically by selective wet etchants, and cannot be etched by conventional RIE. Therefore, a backside etch cannot be adapted to fabricate beam leads for quartz wafers. However, because of its excellent millimeter and submillimeter-wave properties such as low dielectric constant, low loss tangent and good thermal conductivity, quartz is an attractive substrate material for superconducting millimeter- and submillimeter-waveguide circuits.

We developed two topside approaches to beam lead fabrication suitable for whole-wafer processing on quartz chips [6,7]. In both of these processes, after the mixer circuits are completed, trenches are cut along the chip perimeters with a dicing saw. The trenches are diced only partly through the wafer, and to a depth slightly greater than the final chip thickness. The first approach uses a sodium chloride optical flat to planarize a sacrificial epoxy resin within the cut trenches. An oxygen plasma then etches back any excess epoxy atop the quartz chips such that the epoxy becomes planar with the quartz [6]. The second approach relies on a fluid-capillary effect to fill the trenches. It is this second approach that we use for fabricating beam leads on quartz substrates, and discussed in this dissertation [7].

A1.1 Beam Lead Fabrication

The beam lead fabrication process is outlined in Figure 1. The process begins by dicing a set of trenches partially through the quartz substrate, which define the perimeter of the chips. These trenches are then planarized with an epoxy resin. Beam leads are
fabricated across the epoxy-quartz interface. The substrate is then lapped from the backside. Finally, the epoxy is removed, separating the individual chips.

**Figure 1** The beam lead process is outlined by five steps; (1) trench dicing, (2) planarization, (3) beam lead fabrication, (4) backside lapping and finally (5) chip separation.

It is critical that the planarized trenches are level with respect to the substrate surface. In order to fabricate flat beam leads over the trench areas, the sacrificial epoxy must be planar with respect to the substrate surface. The vacuum planarization process ensures that the interface between the substrate and the epoxy is relatively planar. This process produces a continuous interface, which gradually dips 1.6μm across a 140μm wide and 150μm deep trench.

**A1.1.1 Trench Definition**

For our experiments, trenches are defined within a quartz substrate using a wafer-dicing saw. The saw blade (Disco Co., part number NBC-ZH 2050-SE27 HEAE)
produces a kerf width between 35\(\mu m\) and 40\(\mu m\). Multiple overlapping passes with the blade result in trenches that are much wider than the kerf. The exposure of the dicing blade is kept to a minimum in order to maintain blade rigidity. If the exposure is too large, the blade may bend, shifting the cutting edge of the blade into the diced sections of the trench. 150\(\mu m\) deep trenches are diced using a blade exposure of less than 510\(\mu m\), which is the minimum exposure available from the manufacturer.

**Figure 2** The above optical image shows quartz mesas surrounded by 150\(\mu m\) deep trenches. Trench width is around 140\(\mu m\). On the right, along the mesa perimeters are 200nm thick gold structures, upon which are later plated the gold beam leads.

**Figure 3** This photograph of a substrate cross-section shows three diced trenches. Multiple overlapping passes with a dicing saw produce trench widths that are larger than the blade kerf width. In a later step, the trenches are planarized with respect to the tops of the quartz mesas. The ripples at the bottom of the trenches are due to the multiple passes with the dicing saw.
A matrix of diced trenches forms a grid of rectangular mesas surrounded by 150μm deep trenches. Figure 2 shows several of these mesas from a top-down perspective. A cross-section through the substrate, shown in Figure 3, reveals the profile of the mesas and trenches. The trenches extend across the entire wafer to the perimeter of the quartz substrate. In a later processing step, the epoxy is injected into the trenches through these trench openings along the substrate perimeter.

### A1.1.2 Epoxy Planarization

After the trenches are diced, a thin sheet of silicone rubber is laid across the surface of the substrate. Van Der Waals forces cause the silicone to adhere to the tops of the mesas, creating sealed volumes of the trenches. A natural wetting contact eases the application of the silicone; no force is required to seal the silicone to the substrate, and voids are rarely created between the mesa tops and the silicone. The sealed substrate is then placed, bottom side up, onto a specially designed jig, which is shown in Figure 4.

Once sealed and mounted, the jig/substrate is placed into a clear plastic desiccator. Included with the jig is a reservoir of freshly mixed epoxy. The epoxy (Epo-Tek 330) is purchased from Epoxy Technology. The 330 epoxy is a two-component, unfilled epoxy designed for bonding glass fiber optics. The resin and hardener components are mixed in a 10 to 1 ratio by weight. After thorough mixing, the epoxy begins to set. However, the curing process is slow; the epoxy has a pot life of eight hours at room temperature. Curing is accelerated by baking the epoxy to elevated temperatures.

With the substrate and epoxy reservoir loaded, the desiccator is evacuated to approximately 5Torr. During evacuation, the operator holds the desiccator such that the opening in the reservoir is kept above the epoxy. After the chamber is evacuated, the
operator returns the desiccator to a level position, initiating flow of the epoxy. Since the desiccator is made of clear plastic, the operator observes the process and directs the flow of epoxy over the substrate. The epoxy is directed such that the entire backside of the substrate is covered, overflowing the wafer perimeter. The viscous epoxy (360cps at 25C) pours slowly enough for the operator to carefully control the coverage. Approximately 2mL of epoxy is enough to ensure thorough coverage over the perimeter of a 33mm diameter substrate.

Figure 4 The jig used for dispensing epoxy atop the quartz substrate consists of an epoxy dispenser and large metal plates. The plates serve as a large thermal mass, preventing the wafer from heating up too rapidly during the curing bake. The silicone seal is also shown in the image, atop which is a quartz substrate with diced trenches.

After the backside and perimeter of the substrate are thoroughly covered with epoxy, the vacuum within the desiccator is released. The pressure differential between the evacuated trench volume and the atmosphere forces the epoxy into the trenches. Since the trenches extend to the perimeter of the substrate and the silicone rubber only adheres to the top of the substrate, the sealed trenches serve as microchannels though
which the epoxy flows until the entire volume is filled. The epoxy fills the trenches within a few minutes. Afterward, most of the excess epoxy is removed from the backside of the substrate with an eyedropper.

An 80°C bake in an oven cures the epoxy with the silicone rubber still attached to the substrate. The metal block on which the substrate is mounted prevents the substrate and epoxy from heating too quickly. If the temperature of the epoxy ramps up too quickly, variations in the temperature profile across the substrate result in non-uniform curing, which causes cracking of the epoxy within the trenches. After 25 minutes in the oven, the substrate is removed, and the remaining excess epoxy on the backside and around the perimeter of the substrate is gently wiped away with a methanol-soaked static-free swab. The substrate is then returned to the oven and curing is continued for an additional 60 minutes.

To remove the silicone rubber from atop the substrate after curing, the substrate is first mounted to a two-inch silicon carrier wafer with Apiezon-W black-wax. Mounting the substrate to a carrier prevents the wafer from cracking when the silicone rubber is peeled from the substrate. The silicone is then gently peeled away from the substrate, revealing the planarized trenches. Finally, the substrate is removed from the carrier wafer and the black wax is rinsed from the backside with the solvent d-limonene. Figure 5 shows a cross-section of a substrate through several planarized trenches, and Figure 6 shows a top view (SEM micrograph) of several trenches and mesas.
Figure 5 A cross-section through a quartz substrate reveals three trenches planarized with epoxy. Each trench is 140\(\mu\)m wide and 150\(\mu\)m deep. In a later processing step, gold beam leads are fabricated across the epoxy-substrate interface.

Figure 6 The above SEM micrograph shows several quartz mesas surrounded by planarized trenches. Trench width is around 140\(\mu\)m. The sample stage is slightly tilted to reveal discontinuities along the epoxy-substrate interface. The substrate and epoxy are covered with a thin (10nm) layer of sputtered gold in order to improve imaging.

Several problems arise if the epoxy is not cured properly. One problem associated with the curing temperature is rapid out-gassing. If the temperature is too high, rapidly escaping gasses from the epoxy create voids within the trenches that often extend through to the surface. Another issue is warping of the substrate due to stress between the cured epoxy and the substrate. If warping is too severe, cracks may propagate along some of the trench lengths.

Out-gassing, warping and cracking are associated with rapid curing of the epoxy. Rapid out-gassing is avoided so long as the curing temperature is below 160\(^\circ\)C. High
temperature curing schedules (less than 160C, but greater than 100C) performed on a hot plate cure the epoxy within several minutes, but may lead to rapid contraction of the epoxy. If the epoxy contracts too much, considerable stress appears across the substrate, causing the wafer to warp or even crack. Reducing the curing temperature to 80C and performing the cure in an oven over an extended time period eliminates much of this stress. Placing the wafer initially on a cool metal block further minimizes warping by slowing the heating process. Though a slight amount of epoxy contraction still occurs when using a low temperature curing schedule, cracking is completely eliminated.

A1.1.3 Beam lead Fabrication

The beam leads fabricated for this paper vary in thickness from 10μm to less than 2μm, and extend over the trenches by up to 250μm. The beam lead fabrication process begins by depositing a plating seed layer across the entire substrate. A 10nm titanium adhesion layer and a 50nm gold seed layer are deposited by DC magnetron sputtering in a multi-target system with a base pressure of 10^{-8} Torr. After deposition, the substrate is mounted onto a two-inch silicon carrier with black wax, which serves as a ridged support structure for the 250μm thick quartz substrate.

Next, a thick resist is patterned atop the substrate. It is necessary to use a resist that is several microns thicker than the eventual beam lead. For 10μm thick beam leads, a thick positive-tone photoresist, AZ4903, is spun at 2.5krpm for 30 seconds, resulting in a resist thickness of around 15μm. The spinning takes place within an atmosphere filled with PGMEA (propylene glycol monomethyl ether acetate) vapor. The PGMEA environment is created by filling the resist spinner trap with PGMEA, and then covering the trap with a large plastic cover. The presence of the solvent vapor slows the out-
gassing of solvents from within the thick resist. Rapid out-gassing causes cracking to occur within the resist, especially across feature steps. After spinning, the resist is allowed to sit for four minutes within the PGMEA environment plus an additional 30 minutes outside.

After letting the wafer sit for a period, a 15-minute oven bake at 120C cures the resist. Prior to loading into the oven, the substrate is placed on a cooled metal block. The metal block prevents the substrate and epoxy from rapidly heating in the oven, which helps to prevent the thick resist from cracking. Cracking of the resist tends to occur around the epoxy-substrate interface where the coefficients of thermal expansion are discontinuous. If expansion is rapid and non-uniform, the resist will crack, creating voids near the interface through which the plating solution may reach the seed layer. After curing the resist, the block and substrate are removed from the oven and allowed to cool for five minutes at room temperature.

When fabricating beam leads thinner than two or three microns, the photoresist patterns need not be as thick. In place of the AZ4903 photoresist, the thinner photoresist AZ4330 is used; when spun at 3krpm for 30 seconds, the resist thickness is around 4μm. In this case, rapid out-gassing is not an issue so it is not necessary to spin the photoresist in a PGMEA environment. AZ4330 is also not susceptible to cracking, so a simple hot plate bake at 100C for one minute cures the resist.

The beam lead patterns are exposed through a photolithography mask using i-line ultraviolet radiation. Exposure times are 10 minutes for AZ4903 and 0.65 minutes for AZ4330. Power density of the ultraviolet radiation is 7mW/cm². The patterns are developed in AZ400k (diluted 1:4 with de-ionized water). The resists develop in 2.5 to 3
minutes. Finally, an oxygen plasma (50 Watts, 1 Torr, 3 minutes) removes any remaining polymer on the surface of the exposed seed layer gold.

The gold beam leads are platted within the resist patterns using the Techniq-25E gold plating solution. The plating rate is 360nm/min and the plating progress is monitored periodically by measuring the step depth into the resist patterns with a profilometer. The gold is plated to within +/- 0.2\( \mu \text{m} \). Beam leads ranging in thickness from 1.8\( \mu \text{m} \) to 10\( \mu \text{m} \) have been demonstrated.

After plating, the resist is removed with acetone. The exposed gold seed layer is subsequently removed using an iodine-based wet etchant. The titanium adhesion layer is then etched away with BOE (an etchant consisting of hydrofluoric acid and an ammonium fluoride buffer), diluted 10 to 1 with de-ionized water.

After removing the plating seed layer, the quartz substrate is mounted onto a two-inch silicon carrier, with the bottom side of the quartz wafer (non-device side) exposed. The quartz substrate is adhered to the silicon carrier using black wax. The carrier wafer, with the quartz substrate, is then placed onto a lapping system mounting disc, again using black wax. Essential to achieving uniformly thinned chips is starting with a quartz substrate that is level with respect to the silicon carrier wafer. To achieve this, the mounting disc and the carrier wafer are placed in a mounting press. The press is then placed on a hot plate and a pressure of 10psi is applied to the carrier and disc. The press is left on the hot plate until an internal temperature of 120°C is achieved and held for 5 minutes. At 120°C, the black wax melts, allowing the quartz substrate and the silicon wafer to be pressed firmly together. The mounting press is then removed and allowed to cool on a Peltier prior to removing the pressure. Once the mounting press has cooled to
room temperature, the pressure is released, leaving the quartz substrate, silicon carrier and mounting disc uniformly pressed together [8].

The mounting disc is then fitted onto the arm of an Allied High Tech Products Multiprep lapping system. This particular lapping system has a specific parallelism of +/- 2µm over a diameter of 2.25 inches. The backside of the quartz substrate is then thinned using a 30µm grit lapping film. After lapping away approximately 75% of the desired quartz, the 30µm lapping film is removed. The remaining quartz is lapped using 15µm grit lapping film, which leaves a smoother finish on the backside of the quartz chips.

In the final step, the sacrificial epoxy is removed from the trenches. An oxygen plasma, with 200W of power and 1 Torr of pressure, removes the epoxy from the trenches. The high pressure of this etch process ensures an isotropic etch profile, thereby preventing the beam lead from serving as an etch mask for the underlying epoxy. Figure 7 shows a set of completed gold beam leads suspended from a quartz substrate.

Figure 7 1.8µm thick gold beam leads extend from the edge of a quartz substrate in this SEM micrograph. The beam leads were fabricated across an epoxy-quartz interface. In a subsequent step, the sacrificial epoxy was removed with an oxygen plasma, creating the suspended beam leads.
A1.2 Planarization Results

Profilometer plots taken of the epoxy across the trench width indicate the degree of planarization of the epoxy with respect to the mesas. In order to study the planarization process and how it varies from wafer to wafer, a total of 16 profilometer scans of trench profiles were performed on three quartz substrates. Scans were made in roughly the same locations on each substrate. Differences in the placement of the scans from wafer to wafer are no worse than \( \pm 0.5\) mm along the length of the trenches. In Figure 8, the approximate scan locations are shown on a substrate map. Also included in Figure 8 is a photograph of a quartz substrate with planarized trenches. Making many scans across several wafers in consistent locations generates an understanding of how planarization varies across the substrate surface. For all three wafers, the trenches are on average 143\( \mu \)m wide, with a standard deviation of 12.0\( \mu \)m. Substrate diameter is 33mm.

![Planarization of 150\( \mu \)m deep trenches in quartz substrates](image)

**Figure 8** Planarization of 150\( \mu \)m deep trenches in quartz substrates (33mm in diameter and 250\( \mu \)m thick) are studied in this work. Profilometer scans across trenches in 16 locations on three wafers are compared in order to understand the degree of uniformity across each substrate. Above is a photograph of a planarized quartz substrate (right) and a map of approximate scan locations (left). Planarized trenches appear as dark grey lines in the photograph. The dark square in the center of the substrate is the contact pad for the plating jig.

After performing the vacuum planarization process once on each of the three substrates, we find an average maximum dip in the planarization of 3.83\( \mu \)m, with a
standard deviation of 630nm. In Figure 9, a profilometer plot shows the profile of the epoxy across the trench width as it appears after the planarization process. As shown, the epoxy decreases in thickness as the stylus moves further away from the mesas; the maximum height difference between the epoxy and the substrate occurs in the middle of the trench. Given an initial trench depth of 150µm, the trenches are planarized to within 2.6%. However, considering that the gold beam leads later formed atop the epoxy are as thin as 2µm, the 3.8µm dip is considered too large for our beam leads application.

![Epoxy Profile](image_url)

**Figure 9** Performing the vacuum planarization process twice improves planarization. With one fill, the average maximum dip in the epoxy is 3.8µm. After a second fill, planarization is improved to 1.6µm. Given an initial trench depth of 150µm, the final planarization is to within 1.1% of the original depth.

To improve the planarization, the planarization process is repeated once again. In order to facilitate the flow of new epoxy into the trenches, the epoxy is exposed to an oxygen plasma after curing. O₂ plasma (200W, 1 Torr) etches back the epoxy by 30µm to 35µm. The planarization process is then repeated. The dips in the planarization profile are partly attributed to shrinking of the epoxy during the curing process.
Therefore, it is important to minimize the amount of etch-back while still providing enough volume in the trenches through which new epoxy may flow. After the second planarization process, the average maximum dip is reduced to 1.6\(\mu\)m, with a standard deviation of 470nm. Also shown on Figure 9 is a profilometer plot across a trench after a second planarization.

**A1.3 Conclusion**

It is unclear at what thickness quartz chips become too brittle to handle. The chip shown in Figure 10 is between 15 and 20\(\mu\)m thick, and is quite easily handled with a pair of fine-tipped tweezers. However, it is assumed that thinning quartz beyond this thickness will present problems for handling. In addition, the limit of mechanical lapping also approaches a limit; lapping a chip to within a tolerance of several microns with our equipment is simply not possible.

Further investigation into other sacrificial materials is warranted; epoxy is not the ideal planarization material. The Epo-Tek 330 epoxy is not readily removed with a wet chemical etchant or solvent, the curing process conditions must be carefully controlled to avoid cracking and rapid out-gassing, and the oxygen plasma etch for epoxy removal can take several hours to complete. An alternative sacrificial material might better complement the vacuum planarization process. On the other hand, the epoxy is durable enough to withstand the subsequent processing conditions required to fabricate the gold beam leads. In addition, the epoxy molds to the shape of the microchannels very well; the rough epoxy surface shown in Figure 6 is attributed to pitting in the silicone rubber, and not the epoxy itself.
Figure 10 Shown is an SEM micrograph of a quartz chip with gold beam leads and RF filter structures. Inset in the upper right is a close-up of the beam leads. The quartz chip in this image is between 15μm and 20μm thick. The gold beam leads are 3μm thick. The longest beam leads extend from the ends of the chip by 250μm.

A1.4 References


Appendix 2

Equipment List

A2.1 Chemicals

Buffered Oxide Etchant, 10:1, CMOS
Conductive Carbon Paint
Ethylene Glycol, VLSI
Epoxy, Epo-Tek 330 Part A (resin)
Epoxy, Epo-Tek 330 Part B (hardener)
Epoxy, H20E Part A (resin)
Epoxy, H20E Part B (hardener)
Grease, L
Hydrogen Peroxide, 30%, CMOS
N-Methyl-2-Pyrrolidinone, Laboratory Grade
Nail polish, clear
Propylene Glycol USP/FCC
Sulfuric Acid, CMOS
Technic 25 ES Gold Plating Solution
Tetramethyl Ammonium Hydroxide 25% w/w Electronics Grade, 99.9999%
Wax, Black (Wax W)
Wax, Clear (7036, Glyco Phthalate)
Wax, MC-400 (95C)

A2.1.1 Cryogenic Liquids

Nitrogen
Helium

A2.1.2 Developers

Methyl Isobutyl Ketone (MIBK:IPA 1:3), Nano
AZ400K Diluted 1:4
MF-312

A2.1.3 Photo/E-beam Resists

AZ4330
AZ4903
AZ5206
A2.1.4 Reactive Ion Etching Gases

Argon, Ultra High Purity \hspace{1cm} Messer
Dichlorodifluoromethane (CCl₂F₂), 99.0% \hspace{1cm} Messer
Nitrogen, Ultra High Purity \hspace{1cm} The BOC Group
Oxygen, Ultra High Purity \hspace{1cm} Messer
Sulfur Hexafluoride (SF₆), 99.99% \hspace{1cm} Scott Specialty Gases
Trifluoromethane (CHF₃) \hspace{1cm} Messer

A2.1.5 Solvents

Acetone, Electronics Grade \hspace{1cm} Fisher Scientific International, Inc.
d-Limonene, UltraPrep \hspace{1cm} T2 Labs
Isopropanol, HPLC Grade \hspace{1cm} Fisher Scientific International, Inc.
Methanol, Electronics Grade \hspace{1cm} Fisher Scientific International, Inc.
Reagent Alcohol, HPLC Grade \hspace{1cm} Fisher Scientific International, Inc.
Trichloroethylene, Electronics Grade \hspace{1cm} Fisher Scientific International, Inc.

A2.2 Computer Programs

AutoCAD LT 2002 \hspace{1cm} AutoDesk
High Frequency Structure Simulator 8.5 \hspace{1cm} Ansoft Corporation
KaleidaGraph 3.5 \hspace{1cm} Synergy Software

A2.3 Equipment

Aaron’s Cryogenic Dipstick-o-Matic \hspace{1cm} UVaML In-House
Coffee Maker, Brew ‘N Go \hspace{1cm} Black & Decker
Contact Lithography Aligner, KJB 3 (DUV) \hspace{1cm} Suss MicroTec (Karl Suss)
Contact Lithography Aligner, EV 620 \hspace{1cm} EV Group
DC Magnetron Sputtering System (Sputt3) \hspace{1cm} UVaML In-House
DC Magnetron Sputtering System (TriII) \hspace{1cm} UVaML In-House
Dicing Saw, Automatic DAD-2H/6T \hspace{1cm} Disco Corporation
Electron Beam Evaporator, BJD-1800 \hspace{1cm} Temescal
Lapping Machine, Techprep \hspace{1cm} Allied High Tech Products, Inc.
Micromanipulator, 3-axis control \hspace{1cm} Micromanipulator
Microscope, BX60 \hspace{1cm} Olympus
Nanometer Pattern Generation System (NPGS) \hspace{1cm} JC Nabity Lithography Systems
Oxygen Plasma Cleaner, Plasmaline \hspace{1cm} Tegal Corporation
Oxygen Plasma Cleaner, PX-250
Photoresist Spinner
Profilometer, Alpha-Step 200
Profilometer, Dektak 8
 Reactive Ion Etcher, RIE System 1000 TP
 RF Sputterer (TurboSputt)
 SEM, JXA 840A
 SEM, DSM 982 Gemini
 UVO Cleaner, Model 342

March Instruments Incorporated
Headway Research, Inc.
KLA-Tencor
Veeco
The Semi Group, Inc.
UVaML In-House
JOEL
Carl Zeiss International
Jelight Company, Inc.

**A2.4 Evaporator/Sputter Metals**

Gold (Evaporator), Pellets, 99.99%
Gold (Sputt3), 3.0” Dia. Target, 99.99%
Titanium (Evaporator), 3.0” Dia. Target,
Titanium (Sputt3), Pellets, 99.99%
Niobium (Sputt3), 3.0” Dia. Target, 99.95%

Pure Tech, Inc.
Kurt J. Lesker Company
Kurt J. Lesker Company
Cerac, Inc.
Kurt J. Lesker Company

**A2.5 Other Parts**

600 Grit sand paper
Dicing Blade, Diamond, 27HECG or 27HEDG
Gold Standard
Lapping Film, Diamond, 30um Grit Adhesive back
Photomasks, 4”, Quartz
SEM Apertures, 75um, G-A75 - Copper
Silicone Rubber

Disco Corporation
Ernest F. Fullam, Inc.
Allied High Tech Products, Inc.
Microtronics, Inc.
Energy Beam Sciences

**A2.6 Wafers**

Silicon-On-Insulator (SOI) 3um Device Layer
Quartz, 33mm Dia., 250um thick
NbN (Deposited on Soitec SOI)

Soitec
Boston Piezo-Optics, Inc.
Moscow State Pedagogical University
Appendix 3

Publications

The following is a list of publications that were produced as a result of the research presented in this dissertation.

   “Ultra-Thin Silicon Chips for Submillimeter-wave Applications,” Proceedings of the
   15th International Symposium on Space Terahertz Technology, Northampton,
   Massachusetts, April 2004


   “Ultra-Thin SOI Beam Lead Chips for Superconducting Terahertz Circuits,”
   Proceedings of the 6th European Conference on Applied Superconductivity, Sorrento,
   Italy, September 2003

   European Conference on Applied Superconductivity, Sorrento, Italy, September 2003

   Membranes by Vacuum Planarization,” submitted: Journal of Microelectromechanical
   Systems, July 2003


