Machine-Aligned Fabrication of Submicron SIS Tunnel Junctions
Using a Focused Ion Beam

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Abstract—The objective of our research is to develop a machine-aligned technique for the definition and insulation of Nb/Al-AlOx/Nb superconducting-insulating-superconducting (SIS) tunnel junctions with areas as small as 0.2 μm². The fabrication of such ultra-small area planar SIS junctions had previously only been achieved using electron beam lithography (JPL). Typical techniques for the fabrication of micron-scale SIS junctions involve a self-aligned resist lift-off process. The resist pattern is used to define both the junction counter-electrode and the insulation field that separates the wiring layer from the base electrode. The wiring layer contacts the junction counter-electrode through a via in the insulation field that is created during resist lift-off. In our process, the junction is defined and insulated in separate steps; a via through the insulation layer to the junction is aligned and defined using a gallium focused ion beam with nanometer spot-size. Such small area SIS junctions have potential applications in high frequency SIS mixer circuits. They may also be used in experiments to investigate quantum coherence in superconducting circuits and may even serve as the key elements in future superconducting quantum computers.

I. INTRODUCTION

Fabrication of SIS junctions at the University of Virginia has been achieved using a self-aligned resist lift-off process, as represented in Fig. 1. In this process, the junction counter-electrode is defined and insulated using a trilevel resist structure (Fig. 1A). We have found this process to be reliable for fabricating junctions as small as 1.0: μm². However, the trilevel resist process has been much less repeatable for smaller junctions. Extremely small defects in the insulation around the junction perimeter allow leakage currents to bypass the barrier layer. To fabricate SIS junctions smaller than 1.0: μm², we have investigated the use of a Focused Ion Beam (FIB) in our fabrication process. The FIB has allowed us to decouple the junction definition and insulation steps. Decoupling these steps will allow us to 1) use a thinner resist to more accurately define the junction counter-electrode and 2) will insure better insulation of the base electrode from the niobium wiring layer.

Fig. 1. (A) Self-aligned trilevel (Futurex/Nb/Polyimide) sitting atop an unetched SIS junction. (B) SiO shown covering an etched SIS junction.

A. Thinner Resists, Well Defined Junctions

Employing the FIB in our process eliminates the need for a lift-off step to define the via in the insulation layer to the counter-electrode. Typically, to ensure a more reliable lift-off process, it is best to use as thick a resist as possible so that it is easier for the lift-off chemical to get under the material that needs to be removed (Fig. 1B). However, since the resist structure used in the trilevel lift-off process is used both as a lift-off material and to define the counter-electrode, the resist cannot be too thick, or else the definition of the counter-electrode will not be adequate. Therefore, we would like to use as thin a resist as possible in order to accurately define submicron junctions. The self-aligned lift-off process required the use of a thicker than desired resist structure to define the counter-electrodes in order to satisfy the thickness requirements needed to ensure reliable lift-off. Since a lift-off step is not needed for the FIB process, thinner resists can be used to more accurately define sub-halfl-micron SIS junctions.

B. Better Junction Insulation

Use of a trilevel resist structure does not allow for thorough insulation of the sides of the counter-electrode. The proximity of the resist to the edge of the junction causes non-uniform coverage of the insulating material around the junction perimeter. This is attributed to a shadowing effect; the trilevel resist partially blocks the deposition of insulating material close to the junction perimeter as the insulating
material is evaporated onto the wafer. Our new FIB process eliminates this problem by allowing us to deposit a “blanket” layer of insulation over the junctions, thereby ensuring complete insulation of the junction perimeter. By removing the resist structure prior to evaporation of insulating material, we eliminate the shadow effect; actually, the entire junction is covered with insulation. The FIB is then used to form a contact via through the insulation to the top of the junction counter-electrode.

II. THE FOCUSED ION Beam

A FIB extracts and focuses positively charged gallium ions from a liquid metal ion source using a strong applied electric field. The gallium ions are focused onto the specimen surface using two electrostatic lenses. Secondary electrons, produced as a result of the gallium ions striking the specimen surface, are collected and processed to form an image of the scanned area, similar to a scanning electron microscope (SEM). By varying the intensity of the beam and using the scan control mechanisms, the FIB can be used to physically mill patterns into the specimen surface.

Milling patterns are controlled by the user using a computer-aided design (CAD) software interface. The user-defined pattern is broken down into a series of pixels; milling is performed by the FIB one pixel at a time as the beam sweeps across the specimen surface. The dwell time, or the time spent by the beam on one specific pixel, may be controlled by the user. Also, the pixel overlap, or percent each successive pixel overlaps the previous pixel, is also user controllable. Varying the dwell time and pixel overlap allows the user to control the milling process more precisely [1].

III. JUNCTION Definition And Insulation

Since the junction definition and insulation steps are no longer coupled, the need for a trilevel resist scheme has been eliminated. This greatly simplifies the fabrication process by allowing us to use a single layer resist structure to define the junction counter-electrode. However, the resist chosen must withstand the physical and chemical attacks that are present during reactive ion etching (RIE) and wet chemical etching. The negative tone resist, NFR, used for this step was chosen for its ability to withstand these etches.

A. Junction Definition

After forming the resist structures using standard photolithographic techniques, an oxygen cleaning step is performed to clean the Au/Cr-Au layer. Next, an iodine-based wet etch is used to define the Au/Cr-Au layer. Without the oxygen cleaning step, the accurate definition of the Au/Cr-Au layer has been found to be less repeatable. This layer is used to obtain good electrical contact between the junction counter-electrode and the niobium wiring layer without a physical cleaning. The presence of Au/Cr-Au prevents the niobium from oxidizing when exposed to atmosphere [2].

Next, a RIE using a mixture of SF$_6$ (13sccm), CHF$_3$ (10sccm) and N$_2$ (0.4sccm) is used to define the niobium layer. SF$_6$ is a source of fluorine ions, which are highly reactive with niobium. The fluorine-niobium product that is formed is very volatile, making it easily removed from the wafer surface. CHF$_3$ is used to provide carbon and hydrogen in order to induce polymerization. As the etch proceeds, polymers begin to build up on the sidewalls of the junction, thereby protecting the junction from being etched by non-directional fluorine ions [3]. The proportion of CHF$_3$ is controlled such that a thin polymer film builds up on the junction sidewalls where the ion bombardment is minimal but not on the niobium surface where it can inhibit the etch progress.

The RIE of the niobium layer is not as anisotropic as we would desire. When using a polyimide structure or resists such as AZ 4110 to define the junctions, the niobium has always been found to be slightly undercut beneath the Au/Cr-Au layer. However, since switching to the NFR resist, this undercutting problem has been eliminated and our junctions now exhibit anisotropic sidewalls.

B. Junction Insulation and Via Definition

After the junctions are defined, the resist is removed using an oxygen plasma. An insulating layer, either SiO or SiO$_2$ is then deposited onto the wafer in selected areas, including the junction areas. SiO is deposited using a thermal evaporation process while SiO$_2$ is deposited with RF diode sputter-etching. It may also be possible to use a spin-on dielectric as an insulator, which would greatly reduce the time required to insulate the junctions. The insulating layer, which is approximately 200nm thick, sufficiently covers the junctions.

Once the insulation layer is deposited, a 35nm layer of chrome is sputtered on the wafer followed by 5nm of gold. The chrome serves as a metal etch mask used to define the vias through the insulating layer through which the wiring layer will contact the junction counter-electrode. This is represented in Fig. 2A. The chrome mask is then defined using the FIB. Small holes are milled in the chrome directly over the junction sites exposing the insulating material beneath (Fig. 2B). These holes vary in size from 0.09; m$^2$ to 0.25; m$^2$, depending on the size of the junctions below. The location of the vias is determined using CAD software included in the FIB system. By varying the FIB beam current and mill times, the rate and the quality of the milling process can be accurately controlled. The thin gold overlayer prevents the chrome from oxidizing, which could change FIB etch conditions unpredictably.
After the chrome mask is defined using the FIB, the exposed insulating material is etched in an RIE process using 25 sccm of CHF$_3$ and 1.6 sccm of O$_2$. The oxygen is included to break up any polymerization that may occur due to the presence of CHF$_3$. This process is conducted under very low pressure (5mT) to better insure an anisotropic etch. Since the CHF$_3$ etch rate of Cr-Au is approximately ten times slower than that of the insulating layer, the etch selectively stops at the Au/Cr-Au layer. The etch rate of chrome is negligible, which is why chrome is used as the etch mask. A brief cleaning in the RIE is then performed using O$_2$ under high pressure to remove any polymer build up that may have occurred inside the vias during the etch. Fig. 3 shows a completed via, which is now ready for the wiring layer.

**IV. Filling the Vias**

To contact the junction counter-electrode with the wiring layer, the vias must be filled with a conducting material. This has been found to be a problem due to the size of the vias (less than 0.25 mm$^2$). Our standard technique for filling larger vias simply involves sputtering 500nm of niobium over the entire wafer. The niobium easily settles inside the vias, completely filling them without any sort of discontinuities. However, this method is not suitable for smaller junctions because the high aspect ratio (ratio of depth to width) of the smaller vias leads to a relatively large build-up of metal on the via sidewalls. This build-up causes the vias to pinch off, preventing metal from completely filling the vias from the bottom up, leaving a void inside the vias. To circumvent this problem, two techniques for filling vias have been developed. The first technique is a variation of an old process that involves alternately depositing and milling away the niobium wiring layer. The second technique is designed to reduce the aspect ratio of the vias prior to the wiring layer deposition. With a smaller aspect ratio, the vias are more likely to be filled without defect.

**A. Ion Milling, Sputter Deposition**

The first technique involves alternately sputtering and ion milling niobium. An ion milling gun, positioned at 45 degrees with respect to the wafer, is used to mill the vias. Since the gun is positioned at 45 degrees, the ions are not able to reach the bottom of the vias as long as the aspect ratio of the vias is high. Consequently, only the sidewalls of the vias are exposed to the ion flux and the vias are slightly widened at the top. Next, the vias are filled approximately one third full with niobium (about 70nm). SEM micrographs of FIB cross-sections of the vias show that the sidewall build-up of niobium has already become significant at this point and has begun to block metal from reaching the bottom of the vias. The deposition is then halted and the wafer is bombarded by the ion flux for a time such that most all of the previously sputtered niobium has been removed. However, since the ion gun is oriented at a 45 degree angle, the niobium that was deposited at the bottom of the vias remains while the niobium that had been causing pinch-off is removed. This process of deposition and ion milling is then repeated again such that the vias are filled another third of the way and the pinch-off material is removed. Finally, 500nm of niobium is deposited, filling the vias the rest of the way and leaving enough niobium on the wafer surface to define the wiring layer. An SEM micrograph showing a side profile of a via can be seen in Fig. 4. The vias still show small voids at the top, but the size of these voids has been greatly reduced. Further work is needed to completely eliminate the remaining voids. The vias...
have been shown to be able to support the needed supercurrent densities required by SIS junctions with vias as small as 0.16 m². Current-voltage characteristics of a junction fabricated using this technique are shown in Fig. 5.

B. Gold plating

The second technique for filling vias involves gold plating. To begin, all of the junctions are electrically contacted by a temporary wiring layer. The wafer is then mounted on a plating apparatus and submerged in a gold plating solution such that 80nm of gold is plated onto all exposed metal surfaces on the wafer, including the Cr-Au above the junctions. At this point, the vias are partially filled with gold. The aspect ratio of the vias is thereby decreased, making it more likely for sputtered niobium to fill the vias without creating voids. Next, the electrical connections between all of the junctions are removed using the RIE. 500nm of niobium is then deposited on top of the wafer and the wiring layer is patterned using standard photolithographic techniques. The gold plating technique has been shown to be successful for contacting 1 m² SIS junctions with vias as small 0.09 m². A via filled using this technique is shown in Fig. 6.

V. Conclusion

A method for defining submicron SIS junctions has been described. Using the small gallium spot size, anisotropic etching and precise alignment capabilities of the FIB system, a machined aligned insulation technique has been developed. This new process allows for the fabrication of sub half-micron SIS junctions without the use of a complex, trilevel resist structure or electron beam lithography [4]. Two techniques for filling small vias junctions have also been described, both of which show promise for contacting sub half-micron SIS junctions.

REFERENCES
